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Review

Overview of Dual Two-Level Inverter Configurations for Open-End Winding Machines: Enhancing Power Quality and Efficiency

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Abstract: Today, power electronic-based converters are at the core of many modern systems, such as smart grids and electric vehicles. In this context, the Dual Two-Level Inverter (DTLI) supplying an open-end winding machine offers an innovative and promising solution for marine propulsion, aeronautics, and electric vehicles. This configuration provides several advantages, including a reduced DC bus voltage, enhanced fault tolerance, and improved overall system performance. However, ensuring optimal energy efficiency and high-power quality remains a major challenge given the increasing demands for performance and sustainability. This paper presents a state-of-the-art review of the main DTLI configurations and their impact on system performance. Three architectures are analyzed, highlighting their benefits and limitations. This study aims to demonstrate the influence of the DC bus voltage ratio and pulse width modulation strategies on power quality and energy efficiency. The objective is to enhance the understanding of the DTLI's potential and to guide its integration into other electrical systems.

Keywords: dual two-level inverter; open-end winding; power quality; efficiency; common-mode voltage; overcharging DC bus; zero sequence voltage

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1. Introduction

Over the past century, industrial development has significantly contributed to climate change, primarily by increasing greenhouse gas emissions (see Figure 1) [1]. In response to this reality, a global transition towards more environmentally friendly energy sources and less polluting industries has become imperative [2]. In this context, enhancing the quality and energy efficiency of electric drive systems is a crucial factor in the shift towards greener industries. Technological advancements in this field aim to develop more efficient systems that minimize energy consumption and losses while ensuring high levels of performance, reliability, and durability [3]. In recent years, extensive research has been conducted to overcome this technological challenge.

Several studies have focused exclusively on improving power quality. For instance, research in [4] has demonstrated that integrating FACTS devices, such as the Unified Power Quality Conditioner and the Static Synchronous Compensator, can reduce total harmonic distortion (THD) and enhance the stability of modern power distribution grids. Similarly, the study in [5] investigated the implementation of a Dynamic Voltage Restorer to mitigate voltage sags and ensure a stable supply to sensitive loads. Additionally, the

authors of [6,7] analyzed the impact of multilevel inverters on the power quality of wind and photovoltaic systems. The study in [8] examined converter topologies dedicated to high-power electrolysis and their influence on the quality of power injected into AC grids. Furthermore, research in [9–12] proposes a robust control strategy based on sliding mode and fuzzy logic, applied to power electronic converters. This approach aims to enhance the integration of wind turbines and photovoltaic power plants into the grid, enabling them to provide ancillary services while ensuring compliance with grid codes. In addition, studies in [13–15] propose advanced fixed-time sliding mode control strategies combined with nonlinear observers to enhance power quality in microgrid applications. These approaches improve disturbance rejection, ensure fast and robust regulation of the DC-link and output voltages, and enhance the dynamic performance of converters operating within renewable-based hybrid networks. Moreover, studies in [16–18] focus on detecting and diagnosing faulty current sensors to improve power quality by ensuring the stable and reliable control of wind power systems. Finally, research in [19,20] explores high-frequency modeling of electrical machines to design high-performance filters, ultimately improving power quality in the grid.

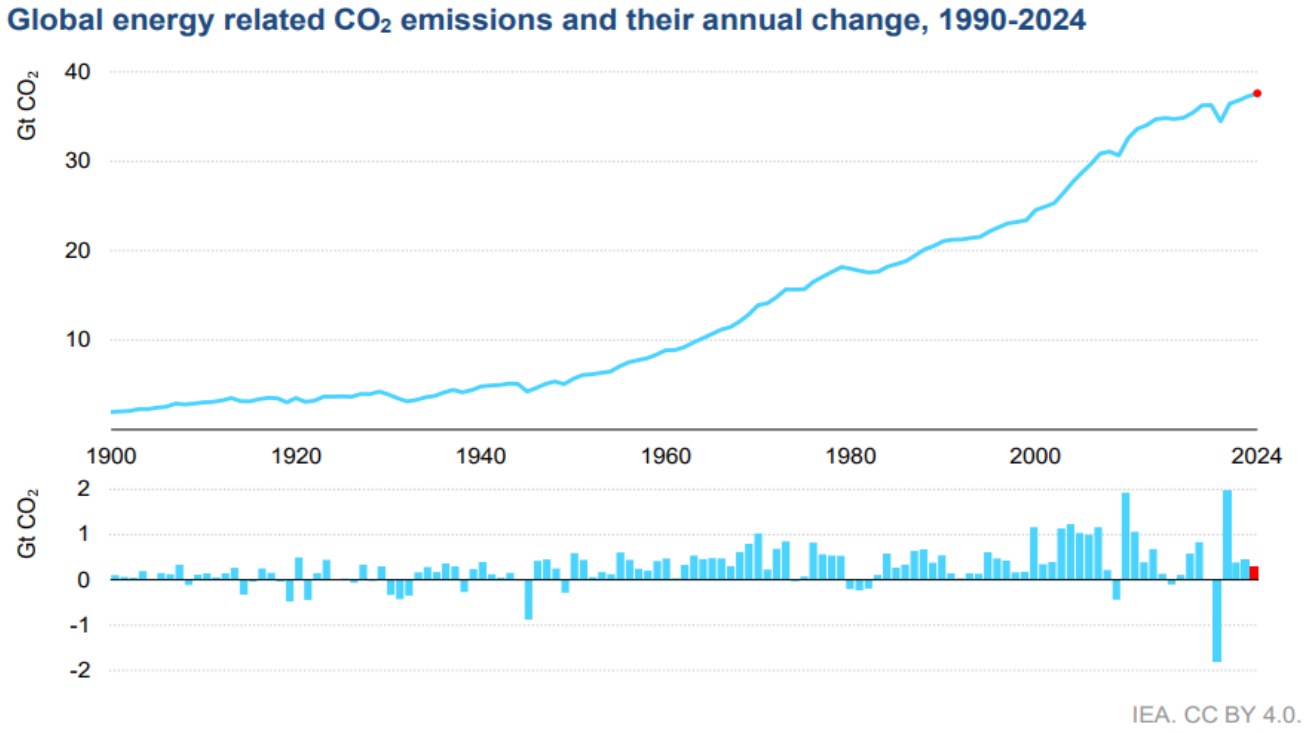


Figure 1. Worldwide greenhouse gas emissions [1].

In the context of improving energy efficiency, several researchers have focused on reducing losses and optimizing energy management to enhance the overall performance of electrical systems. For example, the authors of [21] analyzed asymmetric bidirectional DC-DC converters for power electronic transformers. Their findings demonstrated that these converters reduce peak current and enhance switch safety, thereby optimizing energy efficiency. And the study by [22] proposed the use of a multi-port converter with a high-frequency link for interfacing clean power sources, improving system flexibility and overall efficiency. In addition, the research in [23] introduced a multi-objective approach based on Pareto analysis for Volt/Var control of photovoltaic inverters, enabling the optimized management of reactive power injected into the grid. Other works, such as those in [24–28], have explored advanced power maximization techniques for photovoltaic and wind power

systems. These approaches allow for a more efficient utilization of solar and wind resources while minimizing energy losses.

In the pursuit of simultaneously improving power quality and energy efficiency, research aims to address a major challenge in modern power systems: reconciling performance, reliability, and energy optimization. Studies in [6,29–31] have explored innovative converter configurations to reduce losses, enhance the integration of renewable energy sources, and ensure a high-quality power supply. The integration of NPC multilevel inverters, as investigated in [32], has led to a reduction in THD and power losses, thereby contributing to overall efficiency improvements. Other studies, such as those in [33,34], have introduced advanced inverter architectures designed to optimize both power quality and efficiency in photovoltaic and electric traction systems. Regarding power electronic interfaces, the authors of [35,36] have proposed integrated solutions for electric and plug-in hybrid vehicles, combining an on-board charger and a traction inverter within a unified system. Further research in [37,38] has focused on optimizing multilevel inverters and power electronic converters to enhance the energy efficiency and modularity of electric vehicle charging systems. Additionally, studies in [39,40] have explored the use of cascaded H-bridge inverters and Z-source inverters to optimize electric vehicle performance, extending driving range and improving energy efficiency. Finally, the study in [41] introduces a novel high-performance switched active Z-source inverter topology, demonstrating significant improvements in the lifespan and autonomy of hybrid energy storage systems.

These recent advancements highlight the crucial role of electrical engineering research in enhancing both power quality and energy efficiency while addressing the evolving constraints and demands of modern electrical systems. In this context, increasing attention is being given to a new DC/AC power electronic configuration. Originally proposed by H. Stemmler and P. Guggenbach [42], this topology differs from conventional approaches by isolating the neutral point from the stator windings and arranging two inverters in series, either as two-level or multilevel structures. This design enables independent control of the machine windings through two separate inverters, one for each phase set, leading to what is known as an open-end winding machine driven by a Dual Two-Level Inverter (OEWM-DTLI). The literature identifies three primary power supply configurations for this topology: (i) common DC bus supply (C-DCB) [43,44], (ii) two isolated DC bus sources (TI-DCB) [45,46], and (iii) common DC bus supply with a floating capacitor (DCB-FC) [47,48]. The increasing interest in the DTLI structure is driven by its growing adoption in diverse applications, including electric vehicles [49–52], aerospace [53], and marine propulsion systems [54]. The widespread adoption of this configuration is due to its numerous benefits, including the following:

- The simplicity of the power circuit [55,56].
- The absence of fluctuations in the neutral point [57].
- Enhanced fault tolerance [58].
- Lower DC bus voltage [51].
- A wider operating speed range [59–61].
- The ability to independently control the stator current of each phase [62].
- The potential to achieve a switching frequency that is effectively double, depending on the modulation strategy employed [63].
- The generation of a voltage space vector similar to that of a three-level inverter [64].
- The flexibility to incorporate various energy storage systems on the DC bus of each inverter [65,66].

Nevertheless, it is crucial to recognize that this configuration also comes with certain challenges, such as the following:

- The risk of capacitor overcharging due to unequal DCB voltages in TI-DCB power supplies [67]: this can result in capacitor damage and unwanted harmonics in the motor phase voltage [68].
- The occurrence of zero-sequence voltage (ZSV) caused by the direct coupling of two inverters [69]: this leads to homopolar currents, which generate triple current harmonics [62], adversely affecting motor windings, increasing copper losses, and contributing to circuit saturation [62].
- The presence of common-mode voltage (CMV) resulting from the high-frequency switching of inverter devices [70–72]: CMV creates common-mode currents between the stator phase windings and ground, which can lead to accelerated bearing wear, reducing their service life [73]. Additionally, these currents do not contribute to electromechanical energy conversion and add to the motor's heat losses [74].
- An increase in power losses, due to the greater number of power switches when compared to two-level converters.

It should be noted that each DTLI configuration has a direct influence on performance, complexity, and field of application. Table 1 summarizes the main applications, along with the advantages and disadvantages associated with each type of configuration. In order to fully exploit the potential of these structures and optimize their design, this paper proposes an in-depth state-of-the-art review of the three DTLI configurations and analyzes their impact on system quality and efficiency. To this end, this paper is organized as follows: Section 2 presents the principle of operation of the system under study; Section 3 explores in detail the three DTLI configurations and their specific features; Section 4 analyzes the effect of the DC bus voltage ratio on DTLI performance; Section 5 deals with the control principles applied to this structure; Section 6 discusses the evaluation criteria in terms of quality and efficiency; and, finally, Section 8 summarizes the conclusions of this study.

Table 1. Three different DTLI configurations with their applications, advantages, and drawbacks.

Configuration Type	C-DCB	TI-DCB	DCB-FC
Applications	EV [75], HEV [76], aeronautics [77], start-up generator [78,79], fault-tolerant control [80].	EV systems [81–83], EV in the event of a fault [84], efficiency optimization in EV [85], PV system connected to microgrids [86].	Integrated start/alternator [87], electric aeronautics [88], EV and HEV for a wide speed range [49,89], fault-tolerant control [90].
Output voltage levels	2 [88].	3 ≥ [91].	3 ≥ [91].
Advantages	- No additional hardware required. - Simple control. - Has the highest fault tolerance because it is symmetrical.	- Absence of ZSV. - Greater tolerance to faults.	- Avoid circulation of ZSV. - No isolation circuit required.
Drawbacks	- Presence of ZSV. - Presence of CMV.	- The overcharging problem. - Making the system bulky and increasing costs.	- Less efficient because it charges the capacitor via the motor windings and requires more complex algorithms to balance the capacitor voltage level. - Presence of CMV.

2. Study System Definition and Operating Principle

The basic principle of the DTLI configuration is to supply the stator using two separate inverters instead of coupling it in a star or delta configuration [92,93] (see Figure 2). In this configuration, each side of the stator is powered by a dedicated inverter (see Figure 3). This approach has gained popularity in various modern applications due to its advantages [49–51,53,54].

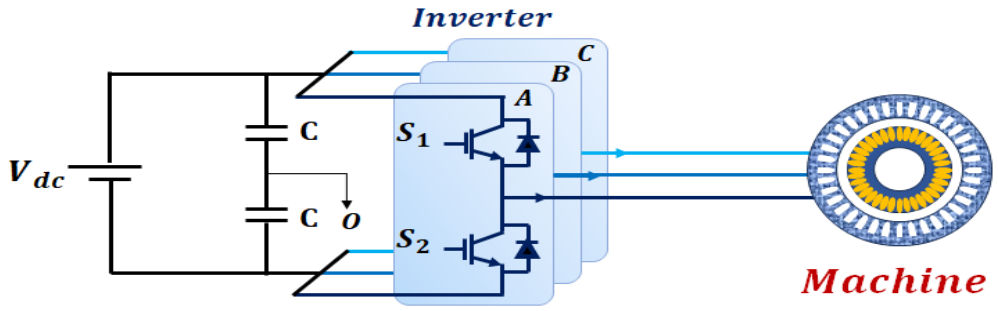


Figure 2. Typical configurations of a star- or delta-connected AC machine.

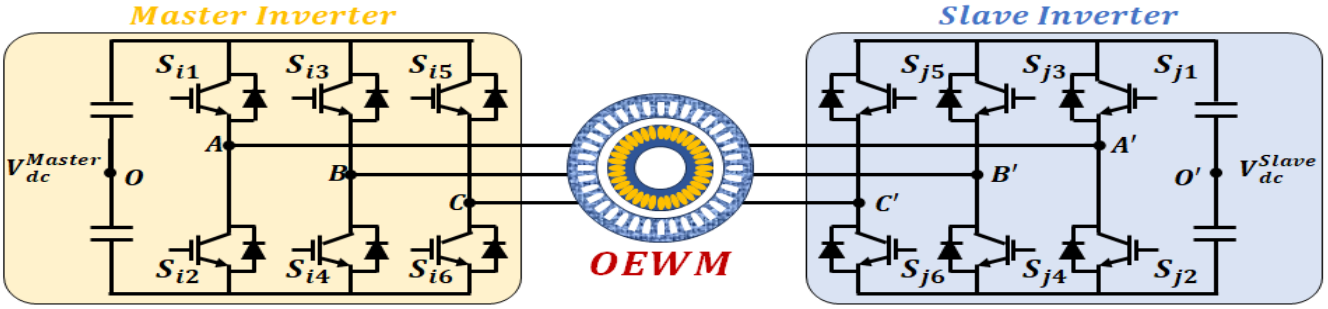


Figure 3. Schematic diagram of machine control with DTLI.

This structure consists of two two-level inverters, referred to as inverter i (Master inverter) and inverter j (Slave inverter), respectively. The voltage vectors in an $\alpha\beta$ reference frame for each inverter (V_i and V_j) can be calculated as follows [94]:

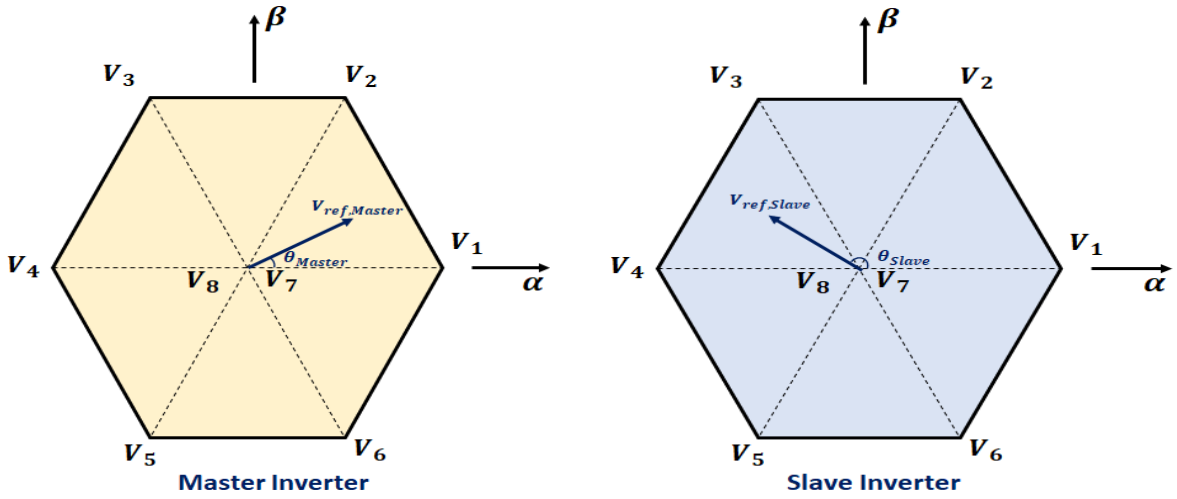
$$V_i = \sqrt{\frac{2}{3}} V_{dc} \left(S_{i1} + \gamma\, S_{i3} + \gamma^2\, S_{i5} \right) \tag{1}$$

$$V_j = \sqrt{\frac{2}{3}} V_{dc} \left(S_{j1} + \gamma\, S_{j3} + \gamma^2\, S_{j5} \right) \tag{2}$$

where $\gamma = e^{j\frac{2\pi}{3}}$, V_{dc} is the DC bus voltage, and S_{i1}, S_{i3}, S_{i5} and S_{j1}, S_{j3}, S_{j5} represent the switching states of inverters i and j, respectively.

As highlighted in the study of [95], the operating principle of the DTLI structure relies on the coordinated synthesis of voltage vectors from both inverters to generate the rotating magnetic field required for motor operation. In a symmetric configuration, when the Master and Slave inverters apply identical voltage vectors simultaneously, their resulting magnetic fields tend to cancel each other out. This cancelation disrupts the formation of the rotating field, potentially causing the motor to stop. To overcome this limitation, asymmetric control strategies are employed. These strategies introduce a phase shift between the voltage vectors generated by the Slave inverter relative to those of the Master inverter, ensuring constructive vector interaction, effective field generation, and sustained motor operation.

Figure 4 illustrates the hexagon formed by the eight voltage vectors generated by Equations (1) and (2). Within this hexagon, each inverter generates six active vectors and two zero vectors. The values “1” and “0” correspond to the on and off states of the inverter switches, respectively.



(**a**) (**b**)

Figure 4. Vectorial diagram of the voltage space of each inverter: (**a**) Master inverter. (**b**) Slave inverter.

Considering the circuits $AA'O'O$, $BB'O'O$, and $CC'O'O$ in Figure 3, the three-phase voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ can be expressed using Kirchhoff's law, as shown in Equation (3):

$$\begin{cases} V_{AA'} = V_{AO} - V_{A'O'} + V_{OO'} \\ V_{BB'} = V_{BO} - V_{B'O'} + V_{OO'} \\ V_{CC'} = V_{CO} - V_{C'O'} + V_{OO'} \end{cases} \tag{3}$$

where V_{AO}, V_{BO}, V_{CO} and $V_{A'O'}$, $V_{B'O'}$, $V_{C'O'}$ represent the three-phase pole voltages of the master inverter and the slave inverter, respectively.

Assuming that the three-phase loads are symmetrical, the sum of the load phase voltages must be zero, as expressed in Equation (3).

$$V_{AA'} + V_{BB'} + V_{CC'} = 0 \tag{4}$$

Thus, $V_{OO'}$ can be obtained by summing the three equations in (3), leading to Equation (5).

$$V_{OO'} = \frac{V_{A'O'} + V_{B'O'} + V_{C'O'}}{3} - \frac{V_{AO} + V_{BO} + V_{CO}}{3} \tag{5}$$

By substituting Equation (5) into Equation (3), the phase voltage expression is updated as follows:

$$\begin{cases} V_{AA'} = \left(\frac{2}{3}V_{AO} - \frac{1}{3}V_{BO} - \frac{1}{3}V_{CO}\right) - \left(\frac{2}{3}V_{A'O'} - \frac{1}{3}V_{B'O'} - \frac{1}{3}V_{C'O'}\right) \\ V_{BB'} = \left(\frac{2}{3}V_{BO} - \frac{1}{3}V_{CO} - \frac{1}{3}V_{AO}\right) - \left(\frac{2}{3}V_{B'O'} - \frac{1}{3}V_{C'O'} - \frac{1}{3}V_{A'O'}\right) \\ V_{CC'} = \left(\frac{2}{3}V_{CO} - \frac{1}{3}V_{AO} - \frac{1}{3}V_{BO}\right) - \left(\frac{2}{3}V_{A'O'} - \frac{1}{3}V_{C'O'} - \frac{1}{3}V_{B'O'}\right) \end{cases} \tag{6}$$

From Equation (6), it can be observed that the phase voltage V_{ij} applied by the DTLI to the OEWM in Figure 2 corresponds to the voltage difference between the two inverters, V_i and V_j. Thus, V_{ij} can be expressed by Equation (7) [96].

$$V_{ij} = V_i - V_j \tag{7}$$

In the power circuit configuration of the three-phase inverters shown in Figure 3, the two switches in each inverter leg operate in a complementary manner, meaning that, when

one switch is turned on, the other is turned off. By utilizing this switching behavior, the phase output voltages of each inverter, referenced to the negative terminal of the DCB, can be expressed in matrix form as follows:

$$\begin{bmatrix} v_{i,A} \\ v_{i,B} \\ v_{i,C} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} S_{i1} \\ S_{i3} \\ S_{i5} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} v_{j,A'} \\ v_{j,B'} \\ v_{j,C'} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} S_{j1} \\ S_{j3} \\ S_{j5} \end{bmatrix} \tag{9}$$

As presented in Equation (7), the phase voltages applied by the DTLI to the OEWM are obtained by computing the difference between the output voltages of the two inverters. This relationship can therefore be modeled by the following equation, which yield

$$\begin{bmatrix} v_{ij} \\ v_{ij} \\ v_{ij} \end{bmatrix} = \begin{bmatrix} v_{i,A} - v_{j,A'} \\ v_{i,B} - v_{j,B'} \\ v_{i,C} - v_{j,C'} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} S_{i1} - S_{j1} \\ S_{i3} - S_{j3} \\ S_{i5} - S_{j5} \end{bmatrix} \tag{10}$$

Based on this principle, the space vector diagram of a DTLI can be represented in Figure 5, where the hexagonal space vector set generated by the slave inverter 'orbits' around the hexagon of the master inverter.

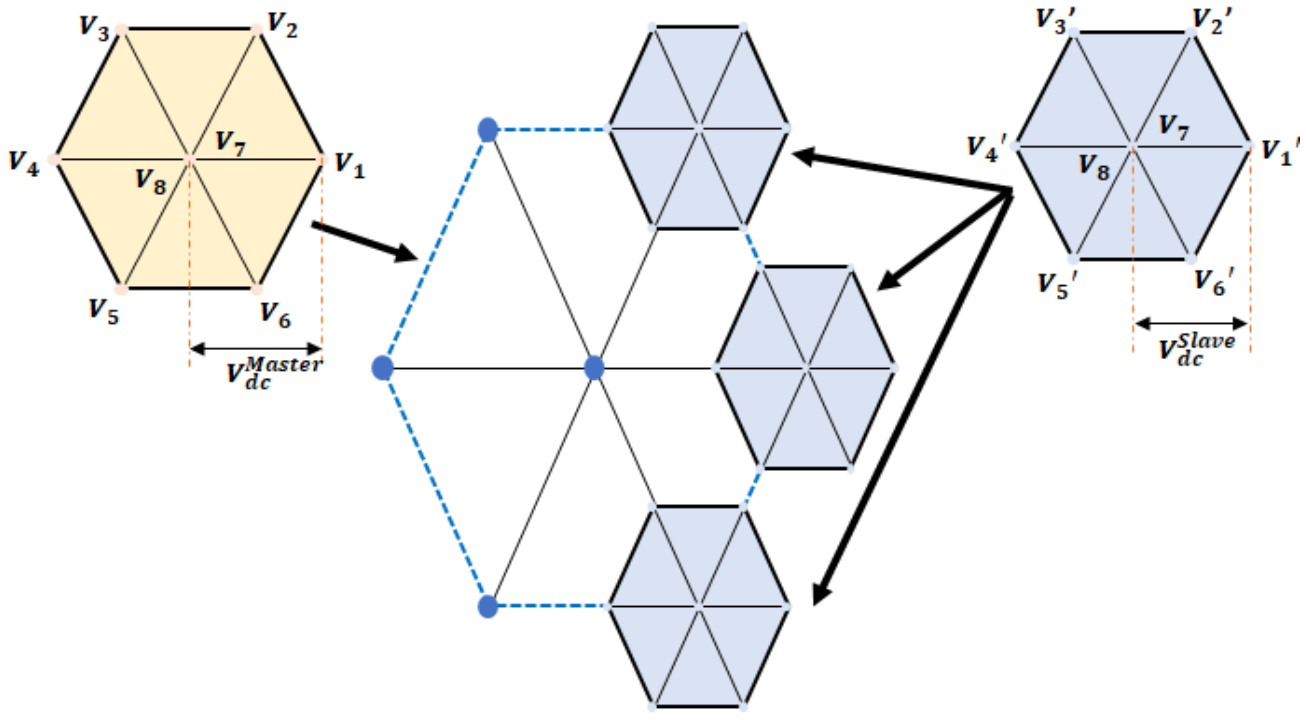


Figure 5. The principle of a space vector diagram resulting from a DTLI.

3. Various System Configurations Studied

In the literature, three different types of system configurations powered by two inverters are identified (see Figure 6): (i) a single common DCB source, (ii) two isolated DCB sources, and (iii) a single DCB source with a floating capacitor.

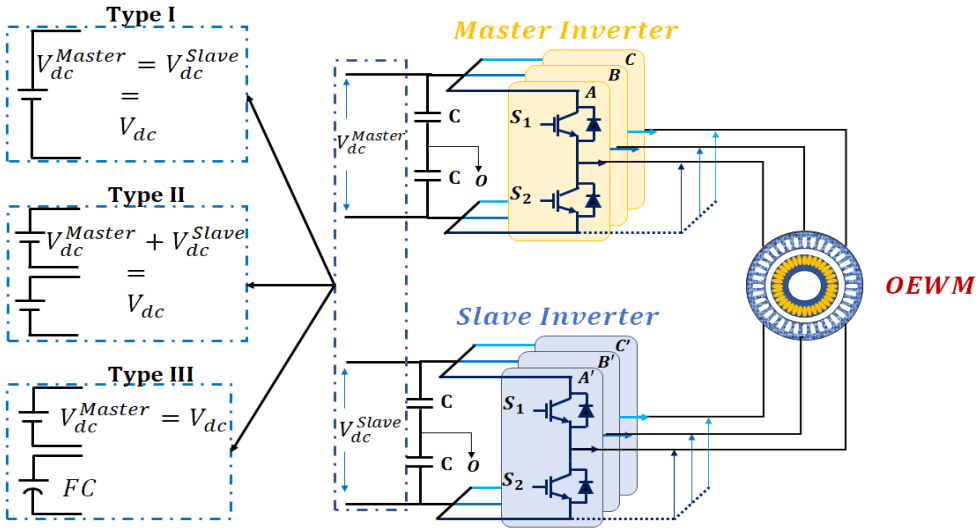


Figure 6. Three types of DTLI configurations for an OEWM.

3.1. Configuration Type I: A Single Common DCB Source

The DTLI drive circuit configuration powered by a single common DCB source (Type I) is shown in Figure 7, where a two-level voltage inverter is connected to each side of the OEWM.

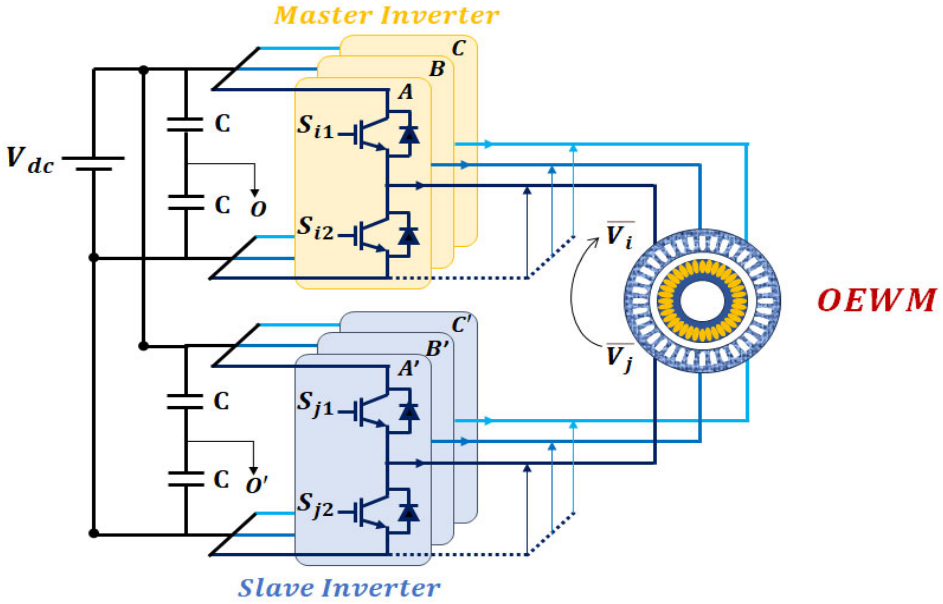


Figure 7. Configuration of a DTLI powered by a common DCB.

Consequently, the DTLI configuration uses twelve semiconductor switching devices (typically IGBTs or MOSFETs) and twelve antiparallel diodes. This configuration relies on the combination of the space vectors from both inverters, resulting in 64 ($2^3 \times 2^3$) possible switching combinations distributed across 19 distinct spatial locations. In this configuration, the set of space vector hexagons generated by the slave inverter 'orbits' around the space vector hexagon of the master inverter. This DTLI configuration is similar to that of a three-level inverter, as shown in Figure 8. It consists of three hexagons with vertices of different lengths: a vertex of length $2/3V_{dc}$ (hexagon ABCDEF), a vertex of length $2/\sqrt{3}V_{dc}$ (hexagon HJLNQS), and a vertex of length $4/3V_{dc}$ (hexagon GIKMPR). Table 2 summarizes the classification of these three hexagons into different vector groups.

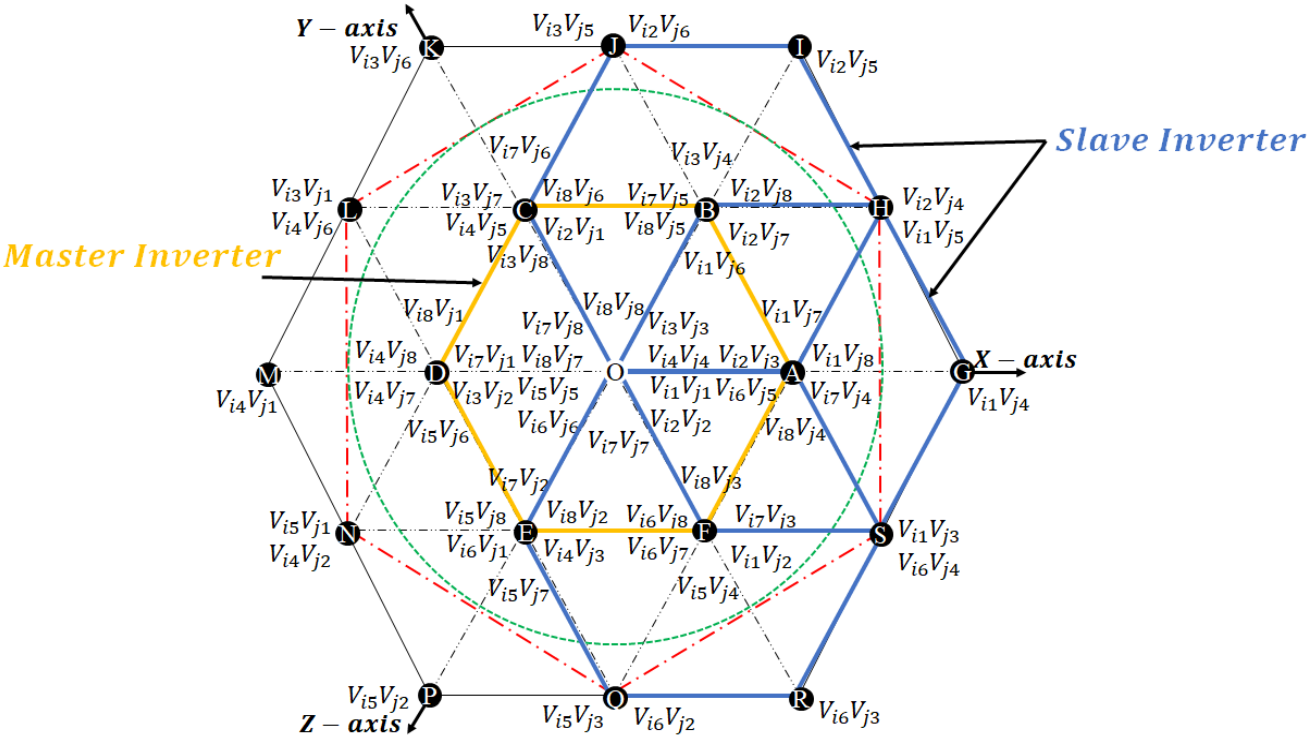


Figure 8. Vector diagram of the space of a DTLI.

Table 2. Voltage vector groups for DTLIs with a common DCB.

Vector Name	N° of Vectors	Magnitude
Zero vectors	O	0
Small vectors	ABCDEF	$2/3V_{dc}$
Intermediate vectors	HJLNQS	$2/\sqrt{3}V_{dc}$
Large vectors	GIKMPR	$4/3V_{dc}$

However, the DTLI configuration powered by a single DC bus source inherently leads to the presence of ZSV, resulting in excessive current and voltage THD. This phenomenon results in high losses, increased temperature, and undesirable vibrations within the machine [97]. Additionally, this configuration is also affected by the presence of CMV.

3.2. Configuration Type II: Two Isolated DCB Sources

This topology is the same as that described in Section 3.1. However, it is based on the use of two isolated DCB sources (Type II), as shown in Figure 9.

This configuration can be divided into two categories: DTLI configurations with symmetrical and asymmetrical voltage sources.

As shown in Figure 9, this configuration features two separate DC buses, which are mutually isolated [55,57,91,96,98–108]. The isolation of the DC buses prevents the circulation of triple-harmonic currents.

The use of the DTLI system, with two DCB sources of unequal values (asymmetrical voltage source), leads to a significant change in the converter operation, compared to the scenario where both DCB sources have equal values (symmetrical voltage source). Figure 10 illustrates the voltage vector generation diagrams for these two cases: one with equal voltage sources and the other with unequal voltage sources $\left(V_{dc}^{Master} = 2V_{dc}^{Slave}\right)$.

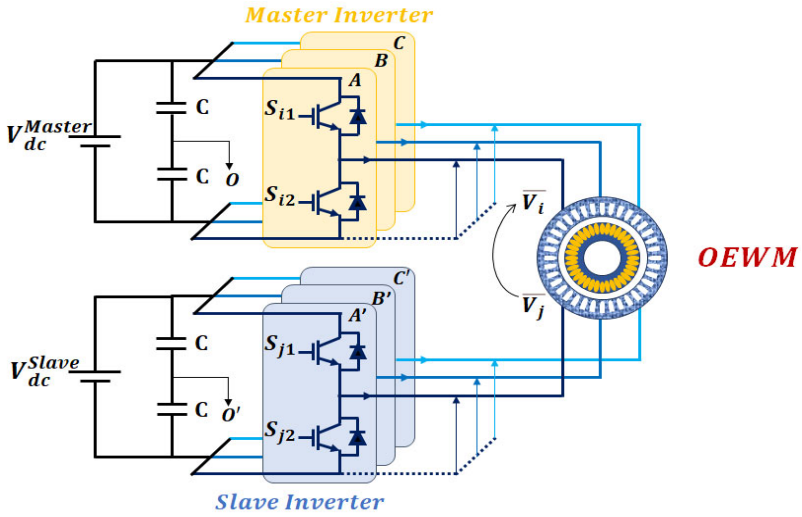


Figure 9. Configuration of a DTLI powered by a two isolated DCB.

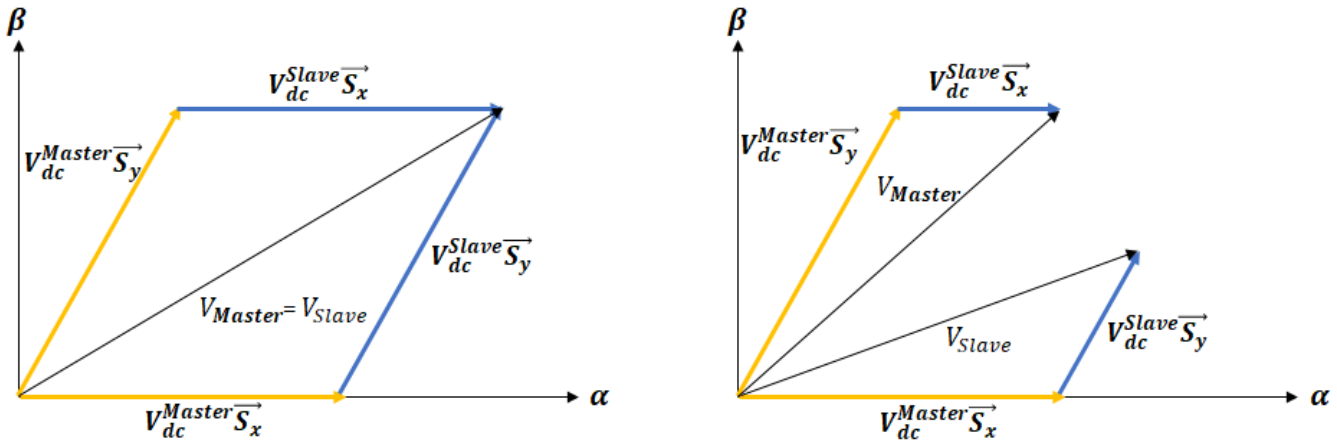


Figure 10. Voltage vector compositions: (**a**) symmetrical voltage source and (**b**) asymmetrical source ratio of (2:1).

The vector voltage diagrams are derived by considering the complex switching sequences S_i and S_j. These sequences are defined for the master inverter $(S_{i1} = 1,\ S_{i3} = 0,\ S_{i5} = 0)$ and for the Slave inverter $(S_{j1} = 1,\ S_{j3} = 1,\ S_{j5} = 0)$, as shown in Figure 3. The output voltages are given by Equation (11), and the corresponding diagrams are provided in Figure 10.

$$\begin{cases} V_i = V_{dc}^{Master}\overline{S_x} + V_{dc}^{Slave}\overline{S_y} \\ V_j = V_{dc}^{Master}\overline{S_y} + V_{dc}^{Slave}\overline{S_x} \end{cases} \tag{11}$$

The complex vectors resulting from various switching combinations are used to indicate the direction of the complex voltage vectors' positions. In this context, there are two voltage vectors: one aligned with the "α" axis and the other 60 degrees out of phase with the "α" axis. The amplitude of the voltage vectors is determined by the electrical source value. If the two voltage sources are of equal intensity, the corresponding voltage vectors will have the same magnitude and orientation. However, if the voltages are unequal, such as in a 2 : 1 voltage ratio, additional vectors are generated. These extra vectors can be observed in Figure 10. Further analysis shows that some of these additional vectors may be redundant. By employing asymmetrical voltage sources, these redundant vectors can

be isolated, increasing the number of available output voltage vectors. This provides a broader range of options for generating distinct output voltages.

Figure 11a illustrates a spatial vector scheme for a two-level DTLI, utilizing voltage sources with an unequal voltage ratio of 2 : 1. This converter system, with a 2 : 1 voltage ratio, generates 37 voltage vectors, which are uniformly and symmetrically distributed in the $\alpha\beta$ plane.

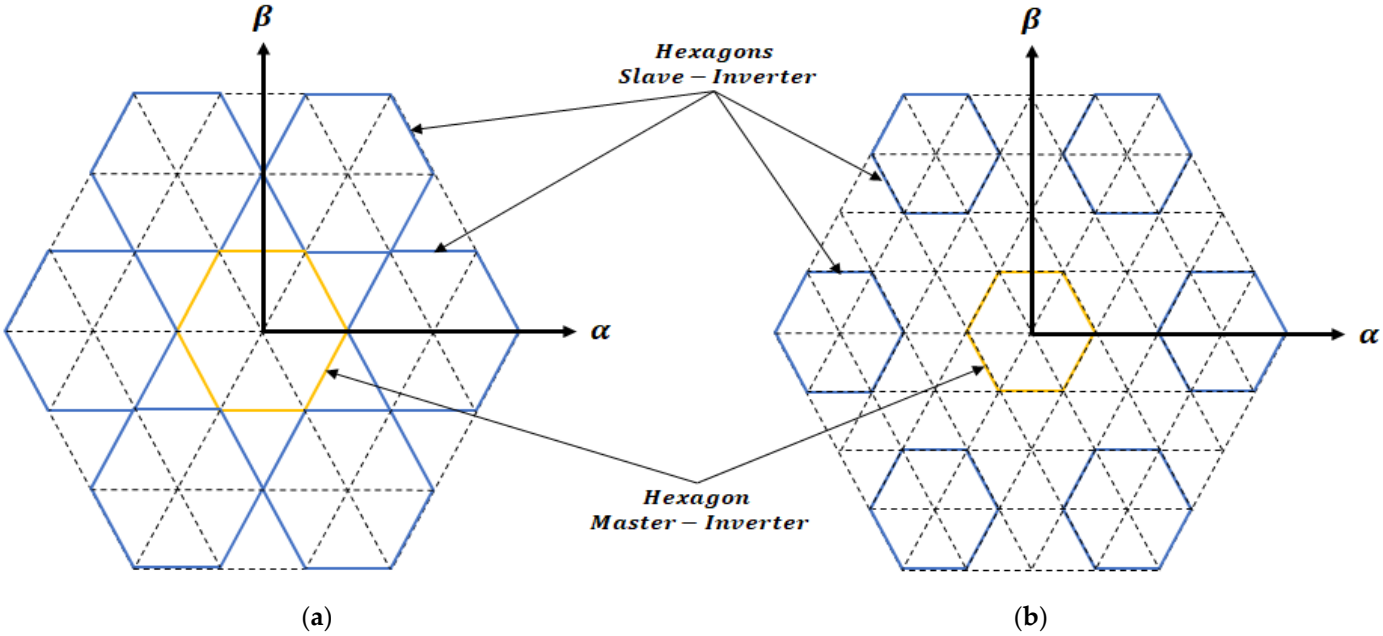


Figure 11. Spatial vector diagram of a DTLI with asymmetrical sources: (**a**) source ratio 2 : 1 and (**b**) source ratio 3 : 1.

On the other hand, the vector diagram shown in Figure 11b is constructed considering the use of asymmetrical sources with a voltage ratio of 3 : 1. In this converter configuration, 48 voltage vectors can be generated. However, these vectors are distributed asymmetrically in the $\alpha\beta$ plane. It should be noted that, in this arrangement, certain areas present challenges regarding the selection of the three closest vectors. This complexity may introduce additional harmonics into the output waveform. Furthermore, in this configuration, the number of redundant states is minimized. As a result, at lower modulation levels, the inverter may cause the overcharging of low-voltage capacitors in specific regions.

The main drawback of this configuration with two iso-linked DC bus sources is the risk of overcharging the DC buses. To prevent this issue, additional components must be integrated.

3.3. Configuration Type III: A Single DCB Source with an FC

This configuration is similar to the one described in Section 3.1. However, a key difference is that, in this structure, the slave inverter is supplied by a floating capacitor (Type III) instead of a DCB source. This distinction is illustrated in Figure 12.

In the DTLI with an FC, as illustrated in Figure 12, the voltage ratio between the DCB sources is defined as $1 : x$, where x is a constant coefficient. In this setup, the master inverter is supplied with a fixed DCB voltage V_{dc}, while the Slave inverter is powered by a floating capacitor that provides a voltage of $x * V_{dc}$. The capacitor is connected without a fixed reference point, and its voltage is naturally self-balanced based on the system configuration and the applied control strategy.

During the modulation process, the phase currents can flow through the FC, resulting in voltage fluctuations across it. By convention, a current flowing into the Slave inverter is considered positive, and the switching states of the Slave inverter directly influence the current through the capacitor.

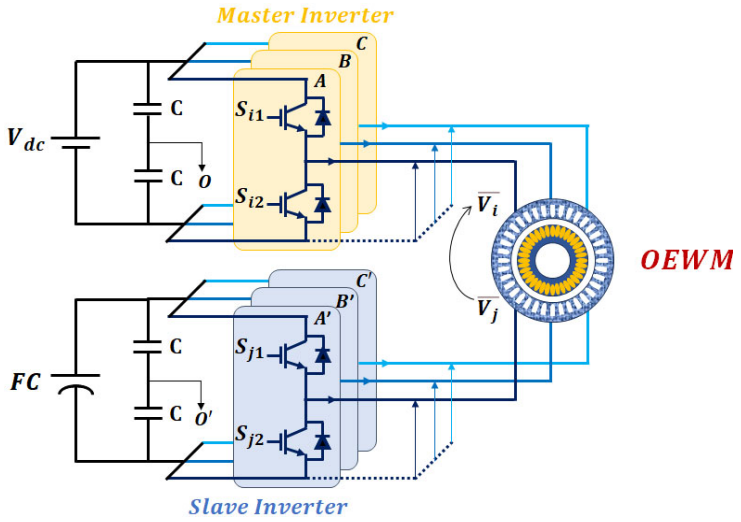


Figure 12. Configuration of a DTLI powered by a single DCB source with an FC.

Since a single modulation vector can be synthesized from multiple switching states, these vectors can be categorized based on their impact on the current flowing through the FC as follows:

- Type 1 vectors: These vectors induce two opposite current flows within the same phase, such as positive and negative currents in phase a, depending on the specific switching states.
- Type 2 vectors: These vectors result in current flow in only one direction within a given phase, for example, only a positive current in phase a.
- Type 3 vectors: These vectors produce no current flow through the FC, regardless of the switching states.
- Type 4 vectors: These vectors generate current flow in different phases, such as a positive current in phase a in one state and a negative current in phase c in another.

This classification offers valuable insight into the interaction between modulation vectors and the dynamic behavior of the FC. A more detailed example of the application of these principles is provided in Section 5.

This configuration combines the advantages of the other two setups, offering multi-level output voltage and voltage amplification capabilities, thanks to the elimination of ZSV circulation. Additionally, it eliminates the need for an isolation circuit, as one of the inverters is floating.

In this DTLI configuration with an FC, the main challenge is regulating the FC voltage to the desired value. Likewise, in DTLI systems with isolated asymmetrical power supplies, a potential concern is that the capacitor on the low-voltage side may be overcharged due to energy flow from the high-voltage side.

In summary, each of the three DTLI configurations presents distinct characteristics in terms of performance, complexity, and implementation requirements. The Type I configuration stands out for its structural simplicity and ease of implementation. However, it is affected by the generation of CMV and ZSV, which can degrade the output voltage quality and increase the overall system losses. The Type II configuration eliminates these undesirable effects and enhances modulation flexibility, especially when asymmet-

ric voltage sources are used. On the other hand, the need for galvanic isolation adds to the cost and increases the risk of capacitor overcharging on the lower voltage side. The Type III configuration offers a good compromise by combining the benefits of the two previous structures while eliminating the need for isolation. Nonetheless, it introduces a challenge in regulating the voltage across the floating capacitor, particularly in transient operating conditions. Therefore, the selection of the most appropriate configuration should be guided by the specific requirements of the application, including cost constraints, control complexity, and desired output voltage quality.

4. DCB Voltage Factor and Ratio

4.1. DCB Voltage Factor

The DCB voltage factor (k) essentially defines the area of the space vector diagram, the inverter's output level characteristics, and the distribution of switching vectors. The area of the space vector diagram limits the maximum utilization of the DC bus voltage, while the level characteristics determine the output quality. It is calculated by dividing the maximum output voltage of a DTLI $V_{ref,max}$ by the DC bus voltage $V_{dc}/3^{1/2}$ in the linear modulation region, as expressed in Equation (12) [48].

$$k = \frac{\sqrt{3}V_{ref,max}}{V_{dc}} \tag{12}$$

4.2. DCB Voltage Ratio

The diagram in Figure 3 shows that the output voltage of a DTLI is essentially the difference between the output voltages generated by the master and slave inverters. Consequently, the ratio between these voltages plays a critical role in shaping the distribution of space vectors in a DTLI. This voltage ratio variation directly affects two key aspects: the area of the space vector diagram and the number of output voltage levels produced by the inverter.

To better illustrate these effects, Figure 13 presents the space vector diagrams of DTLIs for different voltage ratios. As shown, the voltage ratios of 1 : 0.33, 1 : 0.5, and 1 : 1 allow the generation of three, four, and five distinct output levels, respectively. In other words, the selected voltage ratio determines the number of achievable output levels, which directly influences the DTLI's performance characteristics.

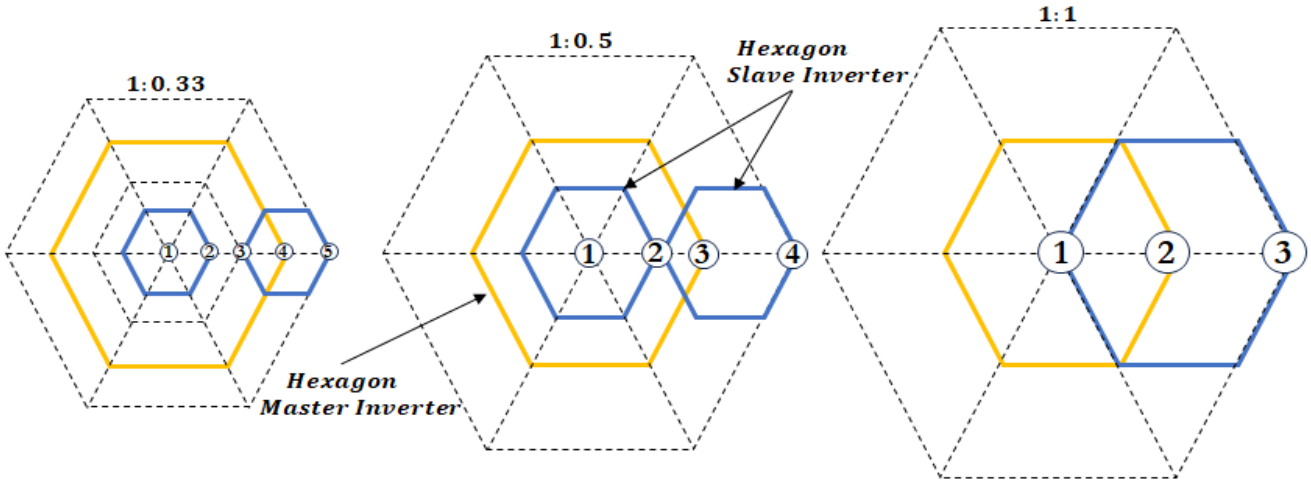


Figure 13. Space vector diagram of DTLIs with different voltage ratios.

5. DTLI Control Features

A review of the existing literature highlights two main modulation strategies applicable to DTLIs: coupled and decoupled schemes [95,105]. These two strategies propose distinct approaches to inverter control and significantly influence the performance of OEWM.

5.1. Coupled Modulation Control

In the case of coupled modulation, a DTLI can be treated as a single multilevel converter. To minimize switching activity, an alternating sub-hexagonal center (SHC) modulation strategy can be implemented, whereby one inverter operates while the other remains in a steady state during a switching period [104,109,110].

Figure 14 illustrates the operation of this alternating SHC modulation technique. The entire space vector diagram is segmented into six regions, each associated with a central SHC point marked by green circles labeled A through F. For each SHC, one inverter performs the switching while the other remains fixed, and then their roles alternate for the subsequent SHC.

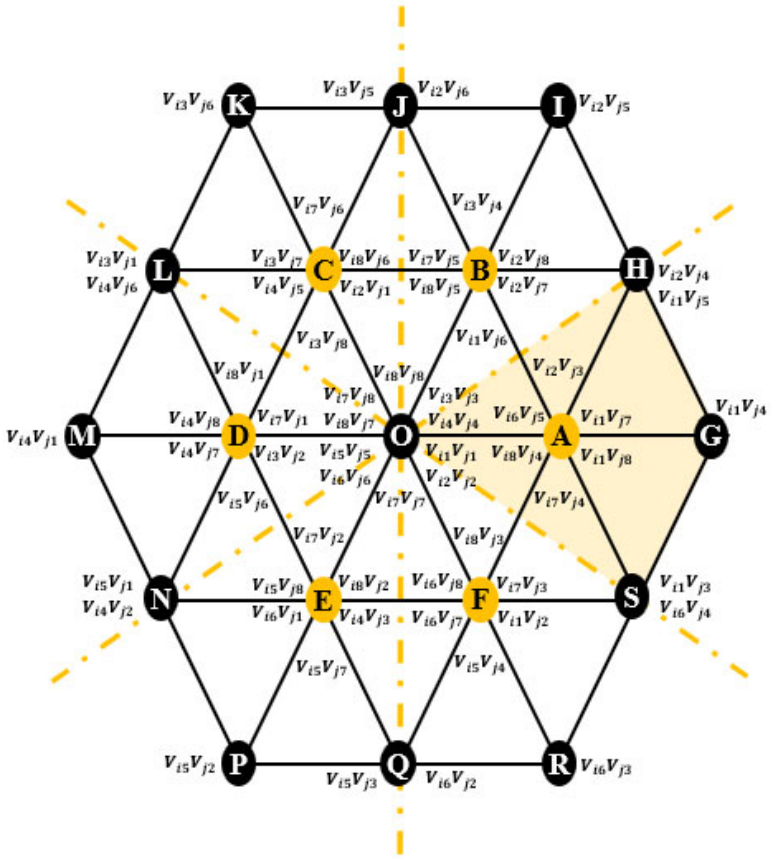


Figure 14. Sub-hexagonal center alternative modulation scheme principle for DTLI.

For instance, point A corresponds to the SHC of the light-green OSGH quadrilateral in Figure 14. Within this region, the switching states can either involve keeping the master inverter fixed at V_{i1} while switching the slave inverter across $V_{i1}V_{j8}$, $V_{i1}V_{j1}$, $V_{i1}V_{j2}$, $V_{i1}V_{j3}$,$V_{i1}V_{j4}$, $V_{i1}V_{j5}$,$V_{i1}V_{j6}$ and $V_{i1}V_{j7}$, or vice versa, holding the Slave inverter constant at V_{j4} and switching the master inverter among states such as $V_{i8}V_{j4}$, $V_{i1}V_{j4}$, $V_{i2}V_{j4}$, $V_{i3}V_{j4}$,$V_{i4}V_{j4}$, $V_{i5}V_{j4}$, and $V_{i7}V_{j4}$.

The authors in [109] conducted a thermal loss analysis of this alternating SHC scheme, demonstrating its impact on system efficiency. Additionally, the authors in [110] showed that this modulation strategy leads to an equal distribution of power losses between the two inverters.

A power-sharing strategy is also defined in [111], taking into account unbalanced power distribution and modulation index values. Moreover, several studies [68,99,112–128] have focused on capacitor voltage regulation for TI-DCB configuration and DCB-FC configuration of DTLIs, respectively.

5.2. Decoupled Modulation Control

As previously mentioned, the output voltage of a DTLI is obtained as the difference between the voltages generated by the two individual inverters.

Under decoupled modulation, the reference voltage V_{ref} is decomposed into two components, namely, $V_{ref,Master}$ and $V_{ref,Slave}$, which are individually supplied to the master and slave inverters, respectively.

This decomposition process is mathematically represented by Equation (13).

$$V_{ref}e^{j\theta_{DTLI}} = V_{ref,Prin}e^{j\theta_{Master}} - V_{ref,Aux}e^{j\theta_{Slave}} \quad (13)$$

The reference vector synthesis diagram is illustrated in Figure 15. Based on Equation (13) and the diagram, it is evident that there are four user-defined parameters, which provide substantial control flexibility that can be strategically exploited.

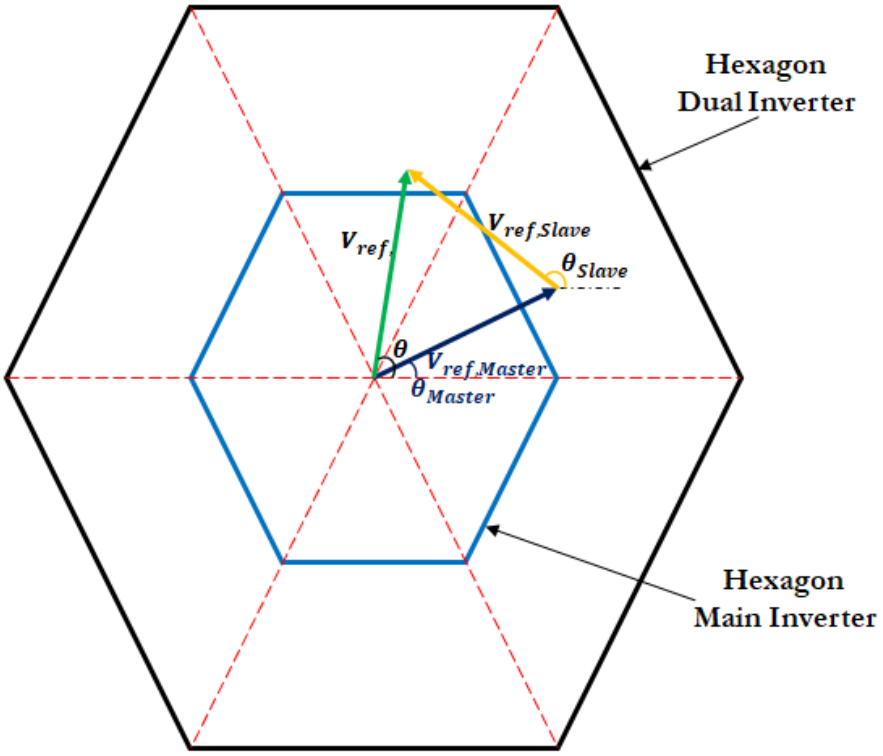


Figure 15. DTLI decoupled modulation principle.

For instance, the authors in [69] adjusted the parameters θ_{Master} and θ_{Slave} to enhance the output voltage profile of DTLIs.

To minimize output current fluctuations, the authors of [96] conducted an analytical study and subsequently proposed a control strategy grounded in decoupled modulation.

Researchers in [67,111,119–126,128–131] focused on capacitor voltage regulation for TI-DCB configuration and the DCB-FC configuration of DTLIs, respectively.

Nevertheless, despite its high flexibility, decoupled modulation introduces undesired voltage steps at the inverter output [119], which can deteriorate the inverter's output performance.

6. Various Criteria for Assessing the Power Quality and Efficiency of the Studied System

The deployment of DTLI configurations offers promising prospects across a wide spectrum of power electronic applications. Nevertheless, each configuration presents a unique set of technical challenges that must be addressed to ensure optimal operation and achieve the desired performance.

In this context, we examine the challenges associated with three distinct DTLI architectures, whose difficulties stem from their specific characteristics, ranging from complex voltage modulation to the management of asymmetrical power sources.

A comprehensive understanding of these constraints is crucial to fully harness the benefits provided by the various DTLI topologies. These challenges can broadly be classified into two categories: those related to power quality and those concerning energy efficiency.

6.1. Power Quality

Electrical power quality has become a critical factor in the design and operation of power systems and electrical machines. This subject has garnered considerable interest from both academic researchers and industrial practitioners, leading to the publication of numerous works in this dynamic and relatively recent field [132].

Power quality encompasses several key issues, such as voltage dips, outages, harmonics (notably THD), over-voltages, unbalances, and voltage fluctuations, among others.

With the introduction of new converter configurations, two additional quality concerns arise: common-mode voltage and zero-sequence voltage.

This study addresses a range of quality-related challenges, including harmonic distortion, common-mode voltage, zero-sequence voltage, DC bus overcharging, and the regulation of floating capacitor voltages.

6.1.1. THD

In systems associated with power converters, output voltage/current quality is closely linked to THD. The IEEE Std 519-1992 standard recommends harmonic control requirements for electrical systems [133].

By definition, THD characterizes the effects of harmonics on power system voltage and can be applied to low-, medium-, and high-voltage systems [133]. The THD is defined by Equation (14).

$$THD_X = \frac{\sqrt{\sum_2^{\infty} X_h^2}}{X_1} \tag{14}$$

where h is the harmonic order, X_h is the amplitude of the harmonic component, and X_1 is the amplitude of the fundamental component.

The IEEE Std 519-1992 standard defines voltage distortion limits at the Point of Common Coupling (PCC) and requires that customers do not introduce excessive current harmonics [133]. For systems where the bus voltage at the PCC is less than or equal to 69 kV, individual voltage distortion must remain below 3%, and the THD must not exceed 5%. The Fast Fourier Transform (FFT) can be used to perform a spectral analysis of electrical signals and thus serves as an effective tool for THD evaluation [134].

6.1.2. Common-Mode Voltage (CMV)

In three-phase sinusoidal power systems, balance and symmetry are fundamental under normal operating conditions. The phase voltages naturally compensate each other, and grounding the source's neutral point reinforces this symmetry.

However, when a three-phase pulse width modulation (PWM) inverter is employed, the switching of asymmetrical voltages introduces a DC voltage (V_{dc}) across the load phases.

This deviates from the ideal sinusoidal behavior, as the instantaneous sum of the load terminal voltages is no longer zero. This deviation leads to the emergence of CMV between the load and ground [135].

CMV results from the high-frequency switching of inverter devices. The common-mode currents induced between the stator windings and ground can have serious consequences, such as premature bearing degradation, increased thermal losses, and an overall decline in motor performance [73].

The CMV generated by the inverter can be expressed by the following equation [136]:

$$V_{cmv} = \frac{1}{3}(V_a + V_b + V_c) \tag{15}$$

In DTLI systems, like the one shown in Figure 5, the CMV for each inverter can be calculated using the formulas provided in the study of [58]:

$$V_{cmv_i} = \frac{S_{i1} + S_{i3} + S_{i5}}{3} V_{dc} \tag{16}$$

$$V_{cmv_j} = \frac{S_{j1} + S_{j3} + S_{j5}}{3} V_{dc} \tag{17}$$

Consequently, the CMV of DTLIs can be calculated as follows [137]:

$$V_{cmv} = \frac{V_{cmv_i} + V_{cmv_j}}{2} \tag{18}$$

$$V_{cmv} = \frac{(S_{i1} + S_{i3} + S_{i5}) + (S_{j1} + S_{j3} + S_{j5})}{6} V_{dc} \tag{19}$$

In the context of DTLI systems, CMV-related issues become more critical due to the frequent high-frequency switching of the inverters' switches. This rapid switching can shorten motor life and increase the risk of inverter failure. Moreover, the impact of these issues is amplified by factors such as shaft voltages, bearing currents, and electromagnetic disturbances caused by common-mode leakage currents [138].

The effects of CMV on the system are primarily influenced by the parasitic parameters between the motor and ground. Among these, parasitic capacitance (C_s) and parasitic resistance (R_b) are crucial in the generation of bearing current, an undesirable component that can negatively affect the system's performance. A schematic diagram (Figure 16) effectively illustrates how these parasitic parameters contribute to bearing current generation in response to CMV.

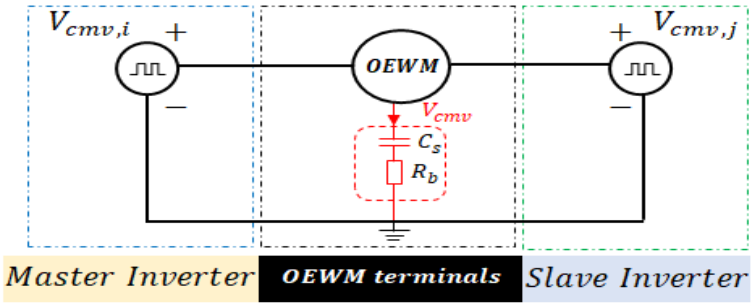


Figure 16. CMV equivalent circuit of an OEWM.

One of the key advantages of a DTLI connection is its ability to attenuate CMV, thereby mitigating the problems associated with it. The combination of spatial vectors resulting from the use of DTLIs leads to a variety of CMV levels, as thoroughly demonstrated in Table 3. From this table, it is evident that large vectors (such as $V_{i1}V_{j4}$, $V_{i2}V_{j5}$, $V_{i3}V_{j6}$, $V_{i4}V_{j1}$,

$V_{i5}V_{j2}$, $V_{i6}V_{j3}$) and zero vectors ($V_{i8}V_{j7}$, $V_{i7}V_{j8}V_{i8}V_{j7}$, $V_{i7}V_{j8}$) effectively eliminate CMV. On the other hand, zero vectors ($V_{i7}V_{j7}$, $V_{i8}V_{j8}$) and intermediate vectors ($V_{i1}V_{j3}$, $V_{i2}V_{j4}$, $V_{i3}V_{j5}$, $V_{i4}V_{j6}$, $V_{i5}V_{j1}$, $V_{i6}V_{j2}$, $V_{i1}V_{j5}$, $V_{i2}V_{j6}$, $V_{i3}V_{j1}$, $V_{i4}V_{j2}$, $V_{i5}V_{j3}$, $V_{i6}V_{j4}$) generate varying levels of CMV.

Table 3. CMV switching vector variations.

N°	Vectors	CMV Levels
1	$V_{i8}V_{j8}$	$-V_{dc}/2$
2	$V_{i1}V_{j8}$, $V_{i3}V_{j8}$, $V_{i5}V_{j8}$, $V_{i8}V_{j1}$, $V_{i8}V_{j3}$, $V_{i8}V_{j5}$	$-V_{dc}/3$
3	$V_{i1}V_{j1}$, $V_{i1}V_{j3}$, $V_{i1}V_{j5}$, $V_{i3}V_{j1}$, $V_{i3}V_{j3}$, $V_{i3}V_{j5}$, $V_{i5}V_{j1}$, $V_{i5}V_{j3}$, $V_{i5}V_{j5}$, $V_{i2}V_{j8}$, $V_{i4}V_{j8}$, $V_{i6}V_{j8}$, $V_{i8}V_{j2}$, $V_{i8}V_{j4}$, $V_{i8}V_{j6}$	$-V_{dc}/6$
4	$V_{i8}V_{j7}$, $V_{i1}V_{j2}$, $V_{i1}V_{j4}$, $V_{i1}V_{j6}$, $V_{i3}V_{j2}$, $V_{i3}V_{j4}$, $V_{i3}V_{j6}$, $V_{i5}V_{j2}$, $V_{i5}V_{j4}$, $V_{i5}V_{j6}$, $V_{i2}V_{j1}$, $V_{i2}V_{j3}$, $V_{i2}V_{j5}$, $V_{i4}V_{j1}$, $V_{i4}V_{j3}$, $V_{i4}V_{j5}$, $V_{i6}V_{j1}$, $V_{i6}V_{j3}$, $V_{i5}V_{j5}$, $V_{i7}V_{j8}$	0
5	$V_{i2}V_{j2}$, $V_{i2}V_{j4}$, $V_{i2}V_{j6}$, $V_{i4}V_{j2}$, $V_{i4}V_{j4}$, $V_{i4}V_{j6}$, $V_{i6}V_{j2}$, $V_{i6}V_{j4}$, $V_{i6}V_{j6}$, $V_{i1}V_{j7}$, $V_{i3}V_{j7}$, $V_{i5}V_{j7}$, $V_{i7}V_{j1}$, $V_{i7}V_{j3}$, $V_{i7}V_{j5}$	$V_{dc}/6$
6	$V_{i2}V_{j7}$, $V_{i4}V_{j7}$, $V_{i6}V_{j7}$, $V_{i7}V_{j2}$, $V_{i7}V_{j4}$, $V_{i7}V_{j6}$	$V_{dc}/3$
7	$V_{i7}V_{j7}$	$V_{dc}/2$

- CMV Reduction

Various approaches have been developed to mitigate CMV, including the use of passive and active common-mode filters [139–142]. However, the implementation of these devices introduces additional costs and significant power losses. As a result, PWM methods have become the preferred solution for two-level inverters, though they do not fully eliminate CMVs [143,144].

In a previous study [145], an approach was presented that exclusively uses even or odd space vector combinations to reduce CMV from $\pm V_{dc}/2$ to $\pm V_{dc}/6$, without relying on null vector states, within a conventional two-level inverter. Additional modulation-based strategies have been developed to eliminate common-mode voltages by using only a specific subset of the output space vectors [146,147]. However, these methods face a limitation regarding the maximum phase voltage, which restricts the optimal use of the DC bus voltage.

6.1.3. Zero-Sequence Voltage (ZSV)

It is widely recognized that unbalanced three-phase voltages can be decomposed into three distinct sets of voltage components [126]. These components, known as "symmetrical components," are classified into positive sequence, negative sequence, and zero sequence. Their schematic representation is shown in Figure 17a. The positive and negative sequence components represent three-phase, rotationally balanced phases, while the zero sequence components correspond to a phase with a zero-phase angle. To provide a clearer understanding of this decomposition, Figure 17b illustrates how an unbalanced three-phase voltage breaks down into its symmetrical voltage components.

Unlike positive and negative sequence currents, zero-sequence currents present a unique challenge. Unlike the former, which compensate for each other, zero-sequence currents add arithmetically at the neutral point of a three-phase, four-wire system. This accumulation can lead to the overloading of the neutral conductor or cause a higher voltage between neutral and earth. Additionally, harmonic currents of any sequence flowing through an AC drive can increase the RMS current, resulting in higher system losses, increased THD for current or voltage, and potential overheating and vibration issues in the machine [135].

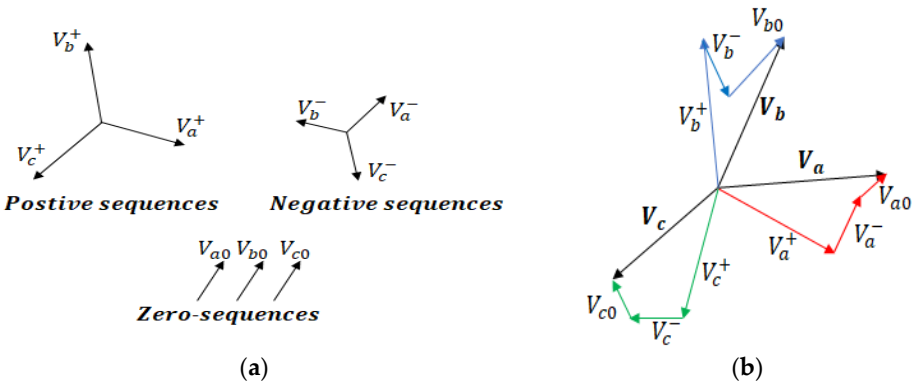


Figure 17. (**a**) Symmetrical components. (**b**) Decomposition of an unbalanced three-phase voltage into symmetrical components.

In a DTLI-powered configuration with a single DCB source, zero-sequence currents (ZSCs) can occur due to ZSV. This voltage arises from the asymmetry of the instantaneous pulse width modulated phase voltages applied to the machine windings, which results from the use of spatial voltage vectors. The corresponding equivalent diagram of the zero-sequence loop is shown in Figure 18. In this diagram, (L_0) represents the inductance of the homopolar sequence, (R) is the resistance of the phase winding, and $V_{cmv,i}$ and $V_{cmv,j}$ are the CMVs generated by the two inverters in the system, respectively.

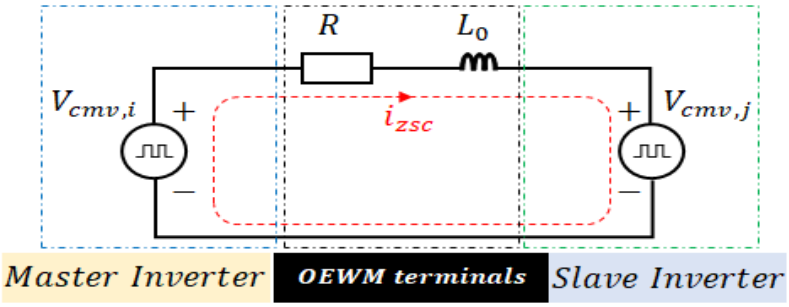


Figure 18. ZSV equivalent circuit of an OEWM.

The ZSV can be expressed in terms of the CMV of each inverter $\left(V_{cmv_i}, V_{cmv_j}\right)$ as follows [62]:

$$V_{zsv} = V_{cmv_i} - V_{cmv_j} \tag{20}$$

$$V_{zsv} = \frac{(S_{i1} - S_{j1}) + (S_{i3} - S_{j3}) + (S_{i5} - S_{j5})}{3} V_{dc} \tag{21}$$

In the DTLI configuration, the ZSV resulting from the 64 space vector combinations can be calculated using Equation (21), as shown in Table 4. From Table 3, it is clear that the zero vectors ($V_{i7}V_{j7}$, $V_{i8}V_{j8}$) and the intermediate vectors ($V_{i1}V_{j3}$, $V_{i2}V_{j4}$, $V_{i3}V_{j5}$, $V_{i4}V_{j6}$, $V_{i5}V_{j1}$, $V_{i6}V_{j2}$, $V_{i1}V_{j5}$, $V_{i2}V_{j6}$, $V_{i3}V_{j1}$, $V_{i4}V_{j2}$, $V_{i5}V_{j3}$, $V_{i6}V_{j4}$) eliminate the ZSV. Conversely, large vectors ($V_{i1}V_{j4}$, $V_{i2}V_{j5}$, $V_{i3}V_{j6}$, $V_{i4}V_{j1}$, $V_{i5}V_{j2}$, $V_{i6}V_{j3}$) and zero vectors ($V_{i8}V_{j7}$, $V_{i7}V_{j8}$) generate various levels of ZSV.

Tables 3 and 4 demonstrate that vectors generating ZSV effectively eliminate CMV. In contrast, vectors designed to eliminate ZSV inevitably introduce CMV. These results highlight the complex interplay between the vectors responsible for both generating and reducing the CMV and ZSV components.

- ZSV reduction

The ZSV issue generates ZSCs, leading to the presence of triple current harmonics [137]. This current can be harmful to motor windings, resulting in increased copper losses and

potential circuit saturation. Several methods have been proposed to eliminate this voltage in DTLI configurations. In [148], the solution involved integrating auxiliary switches, while, in [91], an approach was suggested where one side of the OEWM is fed by a three-level inverter, and the other side is fed by a two-level inverter. However, these solutions require additional hardware, which increases costs. Therefore, a more cost-effective solution would be to design appropriate control strategies to eliminate the ZSV. For instance, in [149], the authors proposed desynchronizing the control between the two inverters to create a 120° phase shift between the voltages of the first and second inverters. Similarly, the authors of [150,151] employed a 180° phase shift and introduced the use of even or odd synchronous vectors. In [152], two approaches were suggested that allow for free selection of DTLI switching states. However, these approaches not only eliminate the ZSV but also restrict the inverter switching. Finally, the authors of [48,153] developed a technique called Decoupled Sample-Averaged Zero-Sequence Elimination, which forces the ZSV to zero while minimizing switching losses. A new method tailored for low switching frequencies, called Synchronous Off-Line Optimum PWM, was presented in [154].

Table 4. ZSV switching vector variations.

N°	Vectors	ZSV Levels
1	$V_{i8}V_{j7}$	$-V_{dc}$
2	$V_{i8}V_{j4}$, $V_{i8}V_{j6}$, $V_{i8}V_{j2}$, $V_{i5}V_{j7}$, $V_{i3}V_{j7}$, $V_{i1}V_{j7}$	$-2V_{dc}/3$
3	$V_{i8}V_{j5}$, $V_{i8}V_{j3}$, $V_{i5}V_{j4}$, $V_{i3}V_{j4}$, $V_{i8}V_{j1}$, $V_{i5}V_{j2}$, $V_{i3}V_{j6}$, $V_{i3}V_{j2}$, $V_{i4}V_{j7}$, $V_{i1}V_{j4}$, $V_{i1}V_{j6}$, $V_{i1}V_{j2}$, $V_{i6}V_{j7}$, $V_{i2}V_{j7}$, $V_{i5}V_{j6}$	$-V_{dc}/3$
4	$V_{i1}V_{j3}$, $V_{i6}V_{j4}$, $V_{i2}V_{j4}$, $V_{i1}V_{j5}$, $V_{i3}V_{j5}$, $V_{i2}V_{j6}$, $V_{i4}V_{j6}$, $V_{i3}V_{j1}$, $V_{i5}V_{j1}$, $V_{i4}V_{j2}$, $V_{i5}V_{j3}$, $V_{i6}V_{j2}$, $V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i1}V_{j1}$, $V_{i5}V_{j5}$, $V_{i4}V_{j4}$, $V_{i3}V_{j3}$, $V_{i2}V_{j2}$, $V_{i1}V_{j1}$	0
5	$V_{i5}V_{j8}$, $V_{i3}V_{j8}$, $V_{i4}V_{j5}$, $V_{i4}V_{j3}$, $V_{i1}V_{j8}$, $V_{i2}V_{j5}$, $V_{i6}V_{j3}$, $V_{i2}V_{j3}$, $V_{i7}V_{j4}$, $V_{i4}V_{j1}$, $V_{i6}V_{j1}$, $V_{i2}V_{j1}$, $V_{i7}V_{j6}$, $V_{i7}V_{j2}$, $V_{i6}V_{j5}$	$V_{dc}/3$
6	$V_{i4}V_{j8}$, $V_{i6}V_{j8}$, $V_{i2}V_{j8}$, $V_{i7}V_{j5}$, $V_{i7}V_{j3}$, $V_{i7}V_{j1}$	$2V_{dc}/3$
7	$V_{i7}V_{j8}$	V_{dc}

6.1.4. DCB Overcharging

DTLI configurations, supplied by two isolated and symmetrical voltage sources (with a voltage ratio of 1 : 1, i.e., both converters use the same voltage level), designed to improve output voltage quality by enabling three-level operation, represented a significant advance in terms of output voltage quality [155].

However, to further improve voltage quality, configurations with two isolated but asymmetrical voltage sources (with a voltage ratio of 2 : 1) were introduced, allowing a four-level operation [67]. However, the use of these asymmetrical sources introduced a potential overcharging problem, particularly at the DC bus capacitor (DCB-C) (see Figure 19).

The overcharging problem is related to the phase current flowing in the DCB-C during the modulation process. This current is made up of the components i_a, i_b, and i_c, as shown in Figure 19. Depending on the specific switching states, these currents can cause the DCB-C to overcharge. To better understand these scenarios, Figure 20 shows different cases of current flow in the DCB-C, using colors to indicate the path of phase current flow. Green represents the i_a current, red the i_b current, and blue the i_c current.

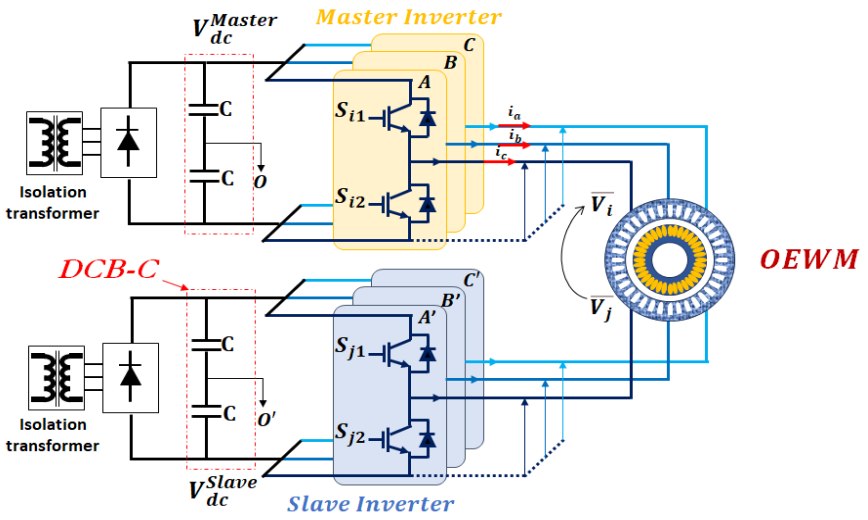


Figure 19. DTLI structure (the overcharging effect).

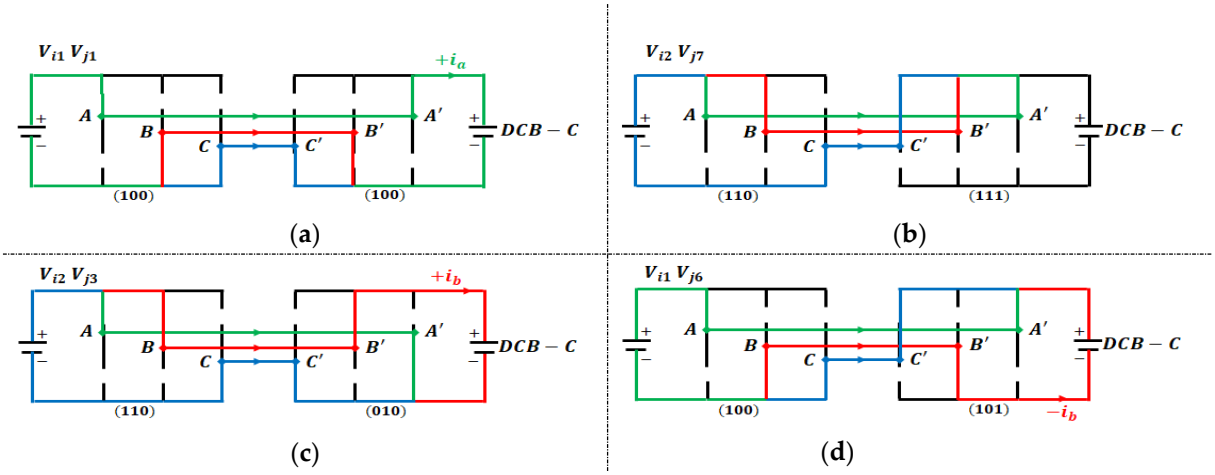


Figure 20. Examples of currents affecting the DCB-C as a function of the switching vectors applied: (**a**) $V_{i1}V_{j1}$, (**b**) $V_{i2}V_{j7}$, (**c**) $V_{i2}V_{j3}$, (**d**) $V_{i1}V_{j6}$.

For example, in Figure 20a, current i_a acts on the positive pole of the DCB-C for the switching state $(V_{i1}V_{j1})$. However, for the switching state $(V_{i2}V_{j7})$, shown in Figure 20b, no current flows through the DCB-C. Figure 20c,d show the current flows resulting from switching states $(V_{i1}V_{j6})$ and $(V_{i2}V_{j3})$, respectively. In the case of the $(V_{i2}V_{j3})$ state, the i_b current flows in the positive polarity of the DCB-C, while, for the $(V_{i1}V_{j6})$ switching state, it flows in the negative polarity of the DCB-C. These currents are referred to as $+i_b$ and $-i_b$, respectively.

- Solving the overcharging problem

When addressing the issue of overcharging in DTLI systems, the literature typically presents two main approaches. The first approach involves adjusting modulation schemes [67,116,118,129,131,156], while the second involves the use of additional hardware [113,117,119,130].

In the first approach, switching states are selected by analyzing the current associated with these states to identify those that are likely to cause overcharging. These problematic states are then avoided during the modulation process. This method of voltage regulation, which assumes the direction of the load current, is referred to as the passive regulation method [157]. However, the disadvantage of this approach is that it reduces the number of vectors available for modulation, which can negatively impact the quality of the output

voltage. A strategy to switch the master inverter while keeping the slave inverter engaged is presented in [118], but this approach involves a larger modulation area, which may result in higher harmonic distortion in the inverter output. To improve power quality, a coupled discontinuous carrier modulation technique is proposed in [129], but this can increase switching losses. A significant limitation of passive control is that it assumes the direction of current, which can be affected by the power factor of the load [157]. An enhanced version of passive control, called active control, was proposed in [156]. This approach actively selects the appropriate states based on control requirements and measured phase current values.

The second approach, which utilizes additional hardware, is based on the nested rectifier–inverter structure proposed in [117] (see Figure 21) and further refined in [158]. In this structure, the slave inverter with a lower DCB voltage is nested inside a higher-voltage DCB feeding the master inverter. This configuration enables the implementation of advanced modulation schemes to optimize voltage utilization for motors [119] or to suppress ZSCs in an averaged manner [130].

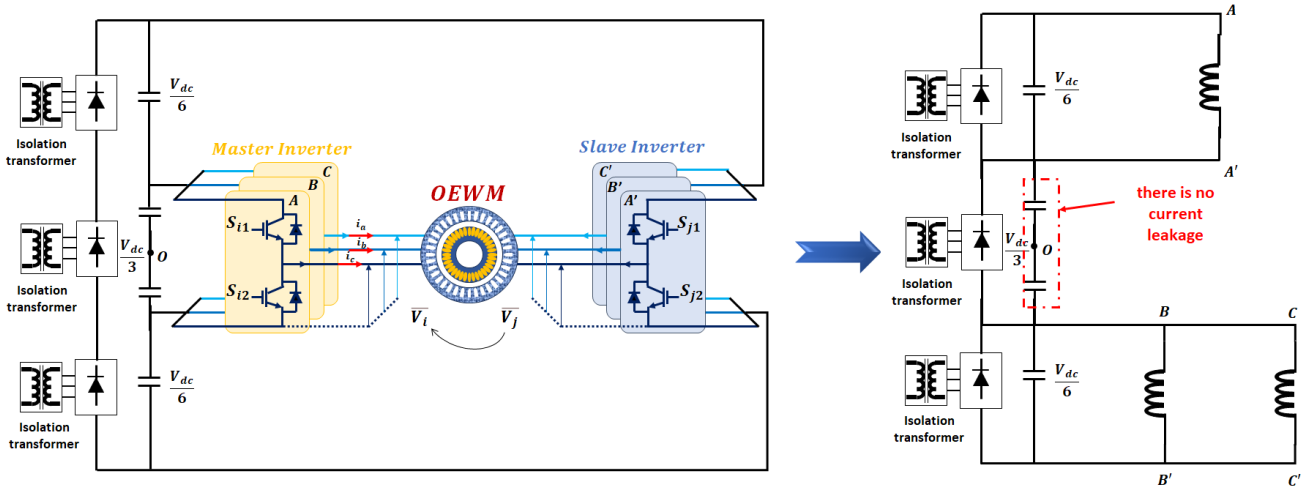


Figure 21. DTLI with a nested rectifier–inverter with OEWM phase connection for the $V_{i1}V_{j1}$ state reported in [117].

It should be noted that, while the nested rectifier–inverter configuration can address the overcharging problem, it requires an additional isolated DC power supply. This addition can lead to increased complexity, size, and cost of the motor drive system [118,129].

6.1.5. Floating-Capacitor (FC) Voltage

Compared to other DTLI configurations, whether with isolated or shared continuous buses, the structure based on a continuous bus and an FC has the notable advantage of minimizing the circulation of ZSVs (ZSCs), which is virtually nonexistent, and does not require additional isolation circuits. However, this approach is not without significant challenges. The main obstacle it faces lies in FC voltage management, which, due to its floating nature [119], generates undesirable voltage steps at the converter output.

As a result of the voltage control approach applied to both converters, the voltage across the load becomes unpredictable. These unwanted voltage steps have the potential to significantly degrade output performance, thereby reducing the attractiveness of this configuration [120]. For example, in the case where the voltage ratio is 1 : 0.5, Table 5 presents the 37 space vectors that will charge or discharge the FC and generate a voltage variation. These vectors can be classified into three types: Type 1 for vectors with redundancy states that cause the phase current to act on both the positive and negative polarities of the FC,

Type 2 for vectors that have only one instance of current flow, and Type 3 for vectors that have no effect on the voltage variation in the FC.

- Maintaining FC voltage

Table 5. Effects of the three types of vectors on current flow in the FC.

Sector	Type 1: Current (±)	Type 2: Current (+ *or* −)	Type 3: No Effects
1	$V_{i1}V_{j1}$, $V_{i8}V_{j4}$, $V_{i7}V_{j4}$, $V_{i2}V_{j2}$, $V_{i8}V_{j5}$, $V_{i7}V_{j5}$, $V_{i2}V_{j3}$, $V_{i1}V_{j6}$	$V_{i1}V_{j4}$, $V_{i1}V_{j5}$, $V_{i2}V_{j4}$, $V_{i2}V_{j5}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i1}V_{j8}$, $V_{i1}V_{j7}$, $V_{i2}V_{j8}$, $V_{i2}V_{j7}$
2	$V_{i2}V_{j2}$, $V_{i8}V_{j5}$, $V_{i7}V_{j5}$, $V_{i3}V_{j3}$, $V_{i8}V_{j6}$, $V_{i7}V_{j6}$, $V_{i3}V_{j4}$, $V_{i2}V_{j1}$	$V_{i2}V_{j5}$, $V_{i2}V_{j6}$, $V_{i3}V_{j5}$, $V_{i3}V_{j6}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i2}V_{j8}$, $V_{i2}V_{j7}$, $V_{i3}V_{j8}$, $V_{i3}V_{j7}$
3	$V_{i3}V_{j3}$, $V_{i8}V_{j6}$, $V_{i7}V_{j6}$, $V_{i4}V_{j4}$, $V_{i8}V_{j1}$, $V_{i7}V_{j1}$, $V_{i4}V_{j5}$, $V_{i3}V_{j2}$	$V_{i3}V_{j6}$, $V_{i3}V_{j1}$, $V_{i4}V_{j6}$, $V_{i4}V_{j1}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i3}V_{j8}$, $V_{i3}V_{j7}$, $V_{i4}V_{j8}$, $V_{i4}V_{j7}$
4	$V_{i4}V_{j4}$, $V_{i8}V_{j1}$, $V_{i7}V_{j1}$, $V_{i5}V_{j5}$, $V_{i8}V_{j2}$, $V_{i7}V_{j2}$, $V_{i5}V_{j6}$, $V_{i4}V_{j3}$	$V_{i4}V_{j1}$, $V_{i4}V_{j2}$, $V_{i5}V_{j1}$, $V_{i5}V_{j2}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i4}V_{j8}$, $V_{i4}V_{j7}$, $V_{i5}V_{j8}$, $V_{i5}V_{j7}$
5	$V_{i5}V_{j5}$, $V_{i8}V_{j2}$, $V_{i7}V_{j2}$, $V_{i6}V_{j6}$, $V_{i8}V_{j3}$, $V_{i7}V_{j3}$, $V_{i6}V_{j1}$, $V_{i5}V_{j4}$	$V_{i5}V_{j2}$, $V_{i5}V_{j3}$, $V_{i6}V_{j2}$, $V_{i6}V_{j3}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i5}V_{j8}$, $V_{i5}V_{j7}$, $V_{i6}V_{j8}$, $V_{i6}V_{j7}$
6	$V_{i5}V_{j5}$, $V_{i8}V_{j2}$, $V_{i7}V_{j2}$, $V_{i6}V_{j6}$, $V_{i8}V_{j3}$, $V_{i7}V_{j3}$, $V_{i6}V_{j1}$, $V_{i5}V_{j4}$	$V_{i6}V_{j3}$, $V_{i6}V_{j4}$, $V_{i1}V_{j3}$, $V_{i1}V_{j4}$	$V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i7}V_{j8}$, $V_{i8}V_{j7}$, $V_{i6}V_{j8}$, $V_{i6}V_{j7}$, $V_{i1}V_{j8}$, $V_{i1}V_{j7}$

The authors in [121,125] addressed the issue of FC voltage regulation in a DTLI while maintaining multilevel operation. Several approaches were examined:

1. Coupled Modulation [121,123–125,128,159]: This method treats the DTLI as a single unit for modulation, enabling analysis of the switching states' impact on the capacitor voltage in steady-state operation. However, there is a risk of under-utilizing the capacitor voltage, which can reduce the output level.
2. FC Voltage Regulation with Reference to Motor Power Factor [121]: This method involves feedback from the motor power factor angle for regulation, providing an active yet complex solution based on motor speed.
3. Decoupled Modulation [65,122,160–163]: In this approach, the FC is treated as a reactive power capacitor, and active power regulation is applied to the FC. However, it may lead to undesirable voltage steps that affect output performance.
4. Step Modulation for the Master Inverter and High-Frequency PWM for the Slave [164]: In this scheme, the master inverter operates at the fundamental frequency, while the slave inverter uses high-frequency modulation. The FC voltage is regulated by adjusting the trigger angle of the fundamental voltage. While this approach reduces switching losses, it may not be suitable for all situations and is relatively complex.

6.2. Energy Efficiency: Power Losses

Generally, there are two types of losses in PWM power electronics converters: conduction losses (P_{cond}) and switching losses (P_{swi}), with switching losses occurring during the transitions from $t_{swi,on}$ to switch-on and from $t_{swi,off}$ to switch-off. These losses are expressed as follows [75]:

$$P_{cond,Sij} = \frac{V_{on,Sij} I_{on} t_{on}}{T_s} \tag{22}$$

$$P_{swi} = \left[\frac{1}{2} v_{swi} i_{swi} \left(t_{swi,on} + t_{swi,off} \right) \right] \times f_{swi} \tag{23}$$

where $i_{swi} = I_{on}$ is the instantaneous phase current, v_{swi} is the switch-off voltage, $t_{swi,on}$ and $t_{swi,off}$ are the switch-on and switch-off times, $V_{on,Sij}$ is the voltage drop, t_{on} is the on-time, and f_{swi} is the switching frequency.

It is well established that, in power semiconductor devices, power losses due to switching are directly proportional to the switching frequency. These switching-related losses occur during the turn-on and turn-off phases of the device and are mainly influenced by the time over which the switching voltage and current rise and fall, respectively [165]. In other words, as the switching frequency increases, the power losses generated by switching also increase. These losses are primarily determined by the variations in voltage and current during these phases.

As an example, Figure 22 illustrates phase A of an inverter arm. In this diagram, components S_{ij}^{+} and S_{ij}^{-} represent the upper and lower switches of the arm, while D_A^{+} and D_A^{-} are the associated antiparallel diodes. Furthermore, Figure 23 shows the voltage across the switch and the antiparallel diode, as well as the current flowing through them and the resulting power losses, particularly when $I_a > 0$.

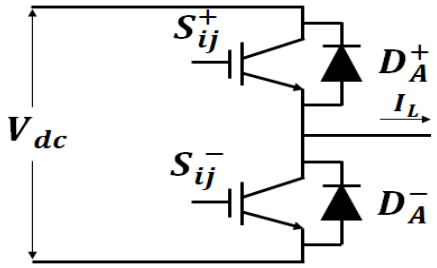


Figure 22. Phase A of the inverter branch.

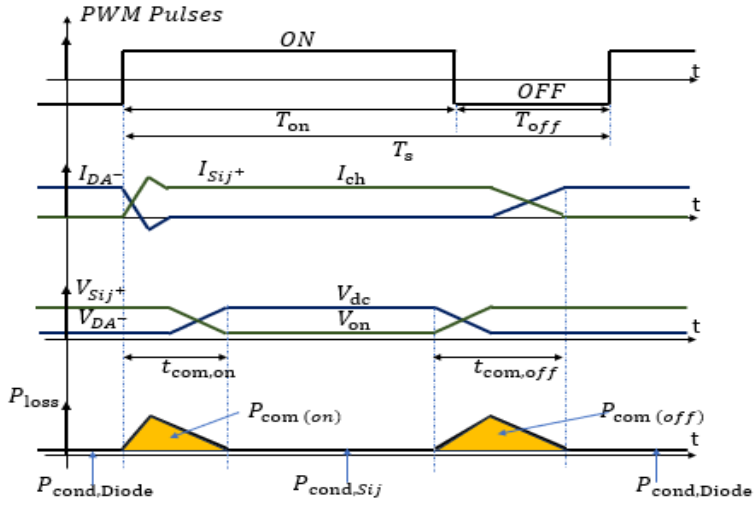


Figure 23. Current through inverter switches and voltage drop between them in phase branch A.

However, the introduction of DTLIs into a system can negatively impact its overall efficiency, primarily due to the increased power losses they generate. In the context of our configuration, it is important to highlight that total switching losses are significantly higher, potentially reaching up to twice the levels observed in conventional systems [97].

- Power loss reduction

To increase the efficiency of DTLI systems, various modulation strategies have been explored in the literature. In references [91,151,152,166], the sub-hexagonal center PWM (SHCPWM) modulation scheme, based on PWM pulse shifting, has been developed to mitigate switching losses. This method involves sequential switching of the two inverters, effectively halving switching losses compared to conventional DTLI configurations. Additionally, SHCPWM avoids the generation of unwanted bearing currents [91]. However, it is limited by a restricted set of switching states and requires complex PWM pulse reordering, which can be computationally intensive [91,151,152,166].

Another approach to minimizing switching losses is discontinuous pulse width modulation (DPWM), as described in [118,167,168]. DPWM holds certain power semiconductors in the ON or OFF position over specific intervals. This technique is more efficient than space vector PWM (SVPWM) for high-power, high-frequency switching applications [59]. Furthermore, different DPWM variants, such as DPWM 30°, 60°, and 120°, have been developed, which reduce switching losses by an average of 33% by avoiding switching

transitions near phase current peaks [169]. DPWM also accounts for the phase difference between current and voltage, even when the power factor is considered [170].

7. Impact of Control Strategies on OEWM-DTLI Performance

As previously mentioned, the OEWM system is powered by a DTLI, and its modeling is similar to that of a conventional AC machine. In terms of control, two complementary levels of strategies can be identified in the literature: high-level control techniques, which focus on the regulation of machine variables (such as scalar control, vector control, and direct torque control (DTC)), and low-level control techniques, which deal directly with the generation of the modulation and carrier signals, typically based on PWM.

Given our focus on voltage quality and energy efficiency, we concentrate on the PWM control of both inverters. Thus, the performance of the OEWM largely depends on how these two inverters are modulated to produce the appropriate output signals.

To provide an overview of the existing literature, Table 6 presents a summary of the three types of configurations studied, highlighting their key contributions and their significant effects on OEWM performance. These contributions are particularly notable for their substantial improvements in critical performance parameters, including overcharging of the capacity, CMV, ZSV, THD, and the efficiency of the DTLI system.

Table 6. Summary of existing contributions on DTLI configurations and their impact on OEWM performance.

DCB Type	REF	Proposed Control Strategy	Improved Performances				
			ZSV	CMV	Overcharging	THD	Efficiency
Type 1	[72]	Proposes the PWM7 strategy, which is based on the combination of switching vectors from groups (3216/3456).	✓	✓	✗	✓	✓
		Proposes the PWM9 strategy, primarily relying on the combination of switching vectors from the (3216/4451) groups.	✓	✓	✗	✗	✗
		Introduces the PWM15 strategy, which relies mainly on the combination of switching vectors from groups (4211/4451).	✗	✓	✗	✓	✗
	[171]	Proposes the use of Zero Sequence Current hysteresis control based on Space Vector Modulation to improve the suppression of parasitic currents and enhance overall system performance.	✓	✗	✓	✓	✗
	[150]	Proposes a carrier-based SVPWM strategy, where the switching duty cycles are calculated using both the measured and reference voltages to improve modulation accuracy and system stability.	✓	✓	✓	✓	✗
	[51]	Proposes a modified SVPWM technique that relies on the application of neighboring vectors, excluding the use of zero vectors, to enhance performance and reduce harmonic distortion.	✓	✓	✓	✓	✓
	[97]	Proposes a generalized discontinuous PWM strategy, which aims to optimize the modulation process by introducing discontinuous patterns to improve the efficiency of the system.	✓	✗	✓	✗	✓
	[172]	Proposes a strategy that decomposes the Zero Sequence Current into two orthogonal continuous signals using orthogonal integral–gate detection technology.	✓	✗	✓	✓	✗
	[131]	Proposes a discontinuous PWM strategy optimized using a genetic algorithm, aiming to enhance the performance and efficiency of the system.	✓	✓	✓	✓	✓
	[80]	Proposes a Fault-Tolerant Control (FTC) method that uses two-phase current sensors when the one-phase current sensor fails while simultaneously suppressing the Zero Sequence Current (ZSC) during post-fault operation to maintain system reliability and performance.	✓	✗	✓	✗	✗

Table 6. *Cont.*

DCB Type	REF	Proposed Control Strategy	Improved Performances				
			ZSV	CMV	Overcharging	THD	Efficiency
Type 1	[173]	Introduces a modified hysteresis torque controller into the direct torque control scheme of a 5-phase open-end winding induction motor, with the goal of enhancing steady-state performance.	✗	✗	✓	✓	✗
	[174]	Proposes a novel PWM strategy for high modulation index regions, aimed at eliminating the Zero Sequence Current component.	✓	✗	✓	✓	✗
Type 2	[156]	Proposes a Nested Inverter Clamped Sample-Averaged Zero-Sequence Elimination PWM strategy, based on the strategic placement of the zero-vector period, and introduces a nested rectifier–inverter circuit design.	✓	✗	✓	✗	✓
	[131]	Proposes a strategy based on unequal reference sharing algorithms utilizing discontinuous PWM and introduces the Coupled Phase Disposition strategy, also based on discontinuous PWM.	✓	✗	✓	✓	✗
	[69]	proposes a near-state Pulse Width Modulation strategy, which focuses on the optimal adjustment of the offset angle and modulation index.	✓	✗	✗	✓	✗
	[117]	Proposes a Sample-Averaged Zero-Sequence Elimination SVPWM strategy, which is based on the adjustment of switching times. Additionally, the work presents a nested rectifier-inverter combination within the conventional two-level inverter configuration, utilizing three DCBs.	✓	✗	✓	✓	✗
	[67]	Proposes a decoupled equal-duty SVPWM strategy, which is based on the use of cycles for all phases.	✓	✗	✓	✗	✗
		Proposes a decoupled proportional-duty SVPWM strategy, which adjusts the duty cycle based on the DCB voltage.	✓	✗	✓	✓	✓
	[113]	Proposes a Decoupled Sampled Average Zero Sequence Elimination strategy, aiming to improve system performance by optimizing zero-sequence current management. Also introduces a power circuit configuration that integrates a rectifier–inverter within a conventional two-level inverter setup.	✓	✗	✓	✓	✗
	[175]	Proposes a new Predictive Current Control strategy, aiming to enhance the dynamic performance and current regulation of the OEWM-DTLI system.	✓	✗	✗	✓	✓
	[176]	Proposes a selection of PWM switching patterns, investigating the effects of continuous PWM, discontinuous PWM, mixed continuous PWM, and mixed discontinuous PWM strategies to enhance the voltage quality and efficiency of the DTLI system.	✗	✗	✗	✓	✓
	[177]	Proposes a class of carrier-based PWM methods in which two phases in each inverter are clamped simultaneously during the entire fundamental cycle, while only one phase switches to generate the reference voltage, aiming to reduce switching losses and common-mode voltage.	✗	✓	✗	✓	✓
	[178]	Proposes a two-stage model-predictive direct torque control scheme designed to balance the state-of-charge of batteries through the appropriate selection of inverter voltage vectors.	✗	✗	✗	✓	✓
Type 3	[125]	Proposes an SVPWM strategy based on five-state switching, avoiding transitions through neighboring vector switching, thereby improving switching efficiency and reducing losses.	✗	✗	✓	✓	✓
	[65]	Proposes a hybrid PWM strategy in which the first inverter is controlled using Six-Step PWM, while the second inverter is controlled using conventional PWM.	✗	✗	✓	✓	✓
	[161]	Proposes a hybrid PWM strategy, where the first inverter uses a PWM method based on a double vector, combining an active vector with an optimal zero vector within a switching period, while the second inverter is controlled by conventional SVPWM.	✓	✗	✓	✓	✓
	[119]	Proposes a floating capacitor voltage regulation scheme based on the use of reference and measured voltages and currents, combined with an improved SVPWM strategy incorporating current feedback and enhancing the exploitation of the converter voltage.	✓	✗	✓	✗	✗

Table 6. *Cont.*

DCB Type	REF	Proposed Control Strategy	Improved Performances				
			ZSV	CMV	Overcharging	THD	Efficiency
Type 3	[47]	Proposes a control scheme based on the optimum selection of voltage ratios, aiming to enhance the modulation performance and improve the voltage utilization of the inverter.	✓	✗	✓	✓	✗
	[179]	Proposes a control scheme based on the decoupling of motor dynamics and floating capacitor behavior, in order to improve system stability and control performance.	✓	✗	✓	✓	✗
	[180]	Proposes a new control scheme aimed at extending the speed range of dual inverter-fed induction motor drives with open-end stator windings.	✗	✗	✓	✗	✗

8. Conclusions

This paper presented a comprehensive technical analysis of Dual Two-Level Inverter (DTLI) topologies for motor drive applications. The investigation covered the fundamental operating principles of DTLI systems and examined three key structural configurations: the conventional Common DC Bus (C-DCB), the Two-Isolated DC Bus (TI-DCB), and the more recent Floating Capacitor-based DC Bus (DCB-FC). A detailed mathematical model of the DTLI system was developed to support this analysis, highlighting voltage distribution mechanisms and control strategies specific to each architecture.

To evaluate system performance, several critical criteria were considered, including total harmonic distortion (THD), common-mode voltage (CMV), zero-sequence voltage (ZSV), energy efficiency, floating capacitor voltage behavior, and the risk of DC bus overcharging. In addition, this study included a comparative summary (Table 6) of several PWM techniques, emphasizing their influence on waveform quality and overall system efficiency across the three configurations.

Among the architectures studied, the dual C-DCB configuration stood out for its simplicity and robustness, attributed to its symmetrical design and straightforward control implementation without the need for additional hardware. However, its limitations in suppressing ZSV, alongside the DC bus overcharging risks associated with the TI-DCB configuration, motivated further interest in the DCB-FC structure. The DCB-FC demonstrated superior performance thanks to its self-regulated floating capacitor voltage and the elimination of isolation requirements.

In conclusion, both the C-DCB and DCB-FC configurations exhibit strong potential for modern high-performance power conversion systems, offering practical trade-offs between simplicity, control complexity, and electromagnetic performance. These findings serve as a foundation for the development of more efficient and reliable inverter systems in future industrial and renewable energy applications.

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Abbreviations

The following abbreviations are used in this manuscript:

DTLI	Dual Two-Level Inverter
DC	Direct Current
AC	Alternative Current
FACTS	Flexible AC Transmission System
THD	Total harmonic distortion

NPC	Neutral Point Clamped
OEWM	Open-end winding machine
FC	Floating capacitor
DCB	Direct Current Bus
C-DCB	Common-Direct Current Bus
TI-DCB	Two Isolated-Direct Current Bus
DCB-FC	Direct Current Bus–Floating Capacitor
ZSC	Zero-sequence current
ZSV	Zero-sequence voltage
CMV	Common-mode voltage
EV	Electrical Vehicle
HEV	Hybrid Electrical Vehicle
PV	Photovoltaic
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SHC	Sub-hexagonal center
PCC	Point of Common Coupling
RMS	Root Mean Square
DCB-C	Direct Current Bus Capacitor
PWM	Pulse width modulation
SVPWM	Space vector pulse width modulation
DPWM	Discontinuous pulse width modulation
SHCPWM	Sub-hexagonal center pulse width modulation

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